POST-GRADUATE EXPERIENCE

by

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for

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This report is in four sections, viz.,

- Research Work & Research Assistantship at Imperial College of Science, Medicine & Technology, London (1982 - 1988).
- Teaching and Administrative Experience in University of Ibadan (1988 to date)
- Teaching and Administrative Experience outside University of Ibadan (1988 to date)
- Major conferences/Workshops attended

Section I: Ph.D. Research Work & Research Assistantship at Imperial College of Science, Medicine & Technology, London (1982 - 1988).

In the course of my Ph.D. research work and research assistantship, I worked extensively on inorganic electron beam resists for integrated circuits fabrication.

Anhydrous cadmium chloride ($CdCl_2$) was used as an electron beam (e-beam) resist for Si/SiO_2 feature fabrication: e-beam decomposition of $CdCl_2$ was followed by dry etching (reactive ion etching) of SiO_2. $CdCl_2$ was chosen as an e-beam resist material because of:

(i) Its e-beam decomposition products, cadmium and chlorine, are volatile at the irradiation temperature

(ii) It has high chemical resistance to fluorine based plasma, and

(iii) Areas not exposed to e-beam irradiation are easily removed.

The decomposition efficiency of $CdCl_2$ film (140nm thick) was found to be $5mC/cm^2$ for irradiation carried out with a 2keV beam, and at a temperature of 210°C. The time, gas flow rate, gas pressure, and r.f. power dependence of etch rates were studied. Selectivity values equal to or possibly much better than 16:1 were achieved in etching SiO_2 compared to $CdCl_2$, and a resolution of 100nm (the order of the film grain size) was obtained.

Lead chloride ($PbCl_2$) and $Pb_{0.8}Cd_{0.2}Cl_2$ films were e-beam irradiated, in order to study the decomposition kinetics and to write metallic and metallic oxide patterns. The decomposition kinetics were studied as a function of temperature, substrate, and current density, by using a quadrupole mass spectrometer to monitor the reaction products, namely cadmium (when appropriate) and chlorine (in all cases). Two classes of reaction mechanisms were used to interpret the results of the decomposition processes in films.

Patterns of Pb, Pb-Cd, and oxidised Pb-Cd were written, but it was found that Pb films were not continuous, while films of Pb-Cd and Pb-Cd oxide were continuous. The pattern resolutions were found to decrease with increasing irradiation temperature. The resolutions of Pb-Cd patterns were found to be superior to those of Pb patterns. The resolution of Pb-Cd and Pb patterns, written at 135°C, were 0.18μm and 0.29μm respectively. Sets of Pb-Cd and Pb-Cd oxide lines, of widths ranging between 0.8 - 3.0μm were written. Ultimate resolution of ~50nm is possible for oxidised Pb-Cd film.

In the course of the above studies, compositional analyses of the samples were carried out by one or more of the following techniques:

(i) Electron Probe Micro-Analysis (EPMA)
(ii) Electron Spectroscopy For Chemical Analysis (ESCA), and
(iii) Secondary Ion Mass Spectroscopy (SIMS)

Surface morphology studies of the samples were performed by Scanning Electron Microscopy (SEM).

The experimental rigs for the Ph.D. research & research assistantship work were in two parts:

(i) the electron beam radiolysis and
(ii) the plasma-assisted etching and end point determination set-ups.

The experimental rigs were extensively adapted for use.

Experimental Set-Up for Electron Beam Radiolysis

The decomposition apparatus is shown in Fig. 1, with all the necessary electronic units used. The arrangement inside the chamber for electron beam radiolysis experiment is shown in Fig. 2, which shows the electron beam deflection plates, the quadrupole mass spectrometer (QMS), and sample manipulator (Fig. 3a) capable of up and down movements, and also with rotation facility. Complete connections and the attachments of the sample holder is shown in Fig. 3b, and clearly visible are the decomposed specimen,

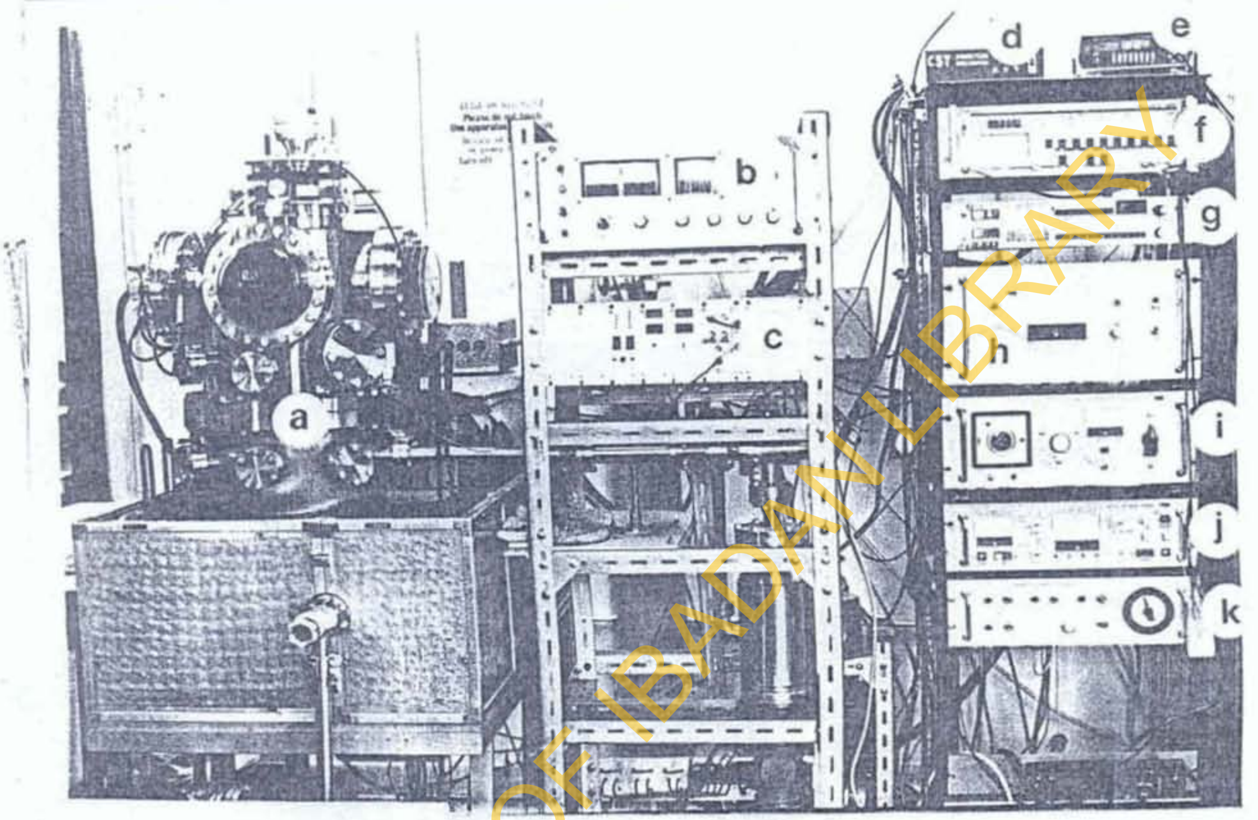


Fig. 1: Electron Beam Decomposition Apparatus

(a) Vacuum chamber
(b) Electron gun power supply
(c) Scanner and Temperature Controller Unit
(d) IEEE 488 Interface
(e) Keithley 480 pico-ammeter; for beam current measurement
(f) EG-G 5205 Lock-in amplifier
(g) SX 300 QMS Controller
(h) ION-pump power supply
(i) Titanium sublimation pump power supply
(j) Pirani/Ion guage control unit
(k) Bake-out heater control

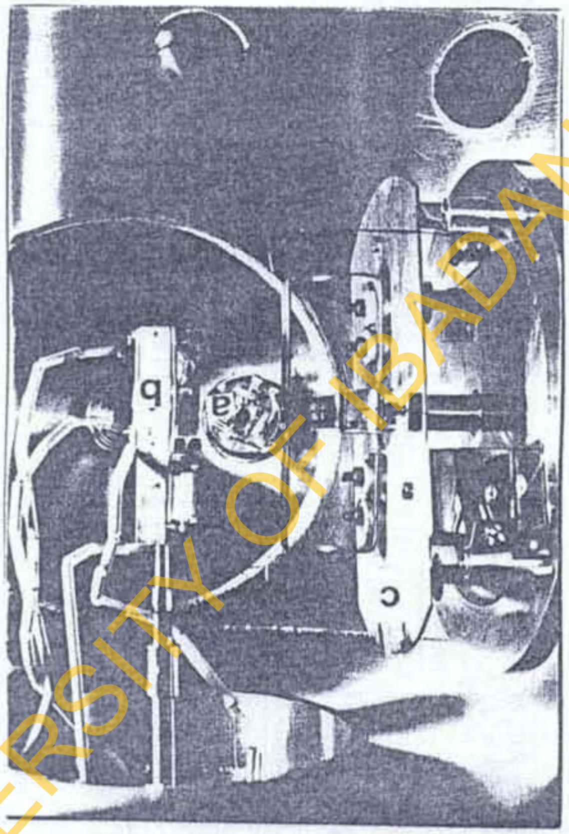


Fig. 2: Lay-out of various components (used for radiolysis) inside the vacuum chamber

(a) Quadrupole Mass Spectrometer

(b) Sample Holder

(c) Electron gun; showing the deflection plates assembly

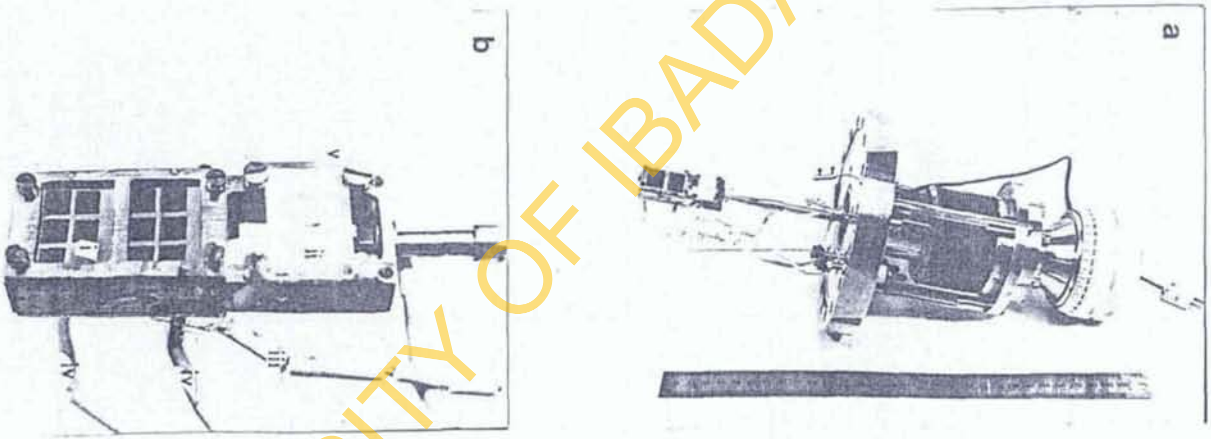


Fig. 3:

(a) Sample Manipulator

(b) Sample Holder:
- (i) Decomposed specimen showing the 4mm x 4mm raster scanned frames
- (ii) Phosphor screen used for e-beam location
- (iii) Thermocouple lead, attached at the back of sample holder
- (iv) Heater connection wires
- (v) Faraday cage, an open rectangular box made with molybdenum for beam current measurement

the phosphor screen, the thermocouple connection, the heater connection, and the Faraday cage for measuring electron beam current. The schematic representation of the electron beam decomposition set-up is as shown in Fig. 4. Decomposition products were detected by using the QMS, and the signal analysed was in synchronism with the electron beam, which is blanked on a 50:50 duty cycle at frequency of 128Hz. In this way, line-of-sight of chlorine (Cl^{35}) and cadmium (Cd^{114}) signals were measured using a lock-in amplifier, which reduces considerably the effect of background signal.

Experimental Set-Up for plasma-assisted etching and end point determination

A small commercial plasma etcher was extensively adapted such that both plasma etching and reactive ion etching (RIE) work could be done, and end-point detection unit using a QMS was added.

The modified equipment used is shown in Fig. 5, and schematically represented in Fig. 6. It is essentially a parallel plate radial flow reactor, that consist of two 18cm diameter water cooled electrodes (made of aluminium), with an inter-electrode spacing of ~3cm. Power was generated by a r.f generator of fixed frequency of 13.56 MHz with the impedance matching (tuning) done manually so as to have minimum reflected power and maximum forward power.

In the plasma mode, wafers were placed on the grounded electrode, known as the anode, and have electrical potential (0V) slightly less than the plasma potential. In the RIE mode, wafers were placed on the powered electrode (the cathode) and has electrical potential with respect to the plasma in the region of about ~-500 to ~-1000V peak-to-peak value.

Vacuum in the etching chamber was achieved by using a rotary pump (installed with a fore-line trap) capable of a base pressure of ~10^{-4} torr prior to introduction of etching gas. The chamber pressure was monitored using a tensioned diaphragm gauge (MKS baratron Type 222). The QMS used, is capable of detecting mass to charge ratio from 1 to 200 a.m.u . The QMS head column was maintained at pressure of 10^{-7} torr during effluent gas sampling by using an ion pump.

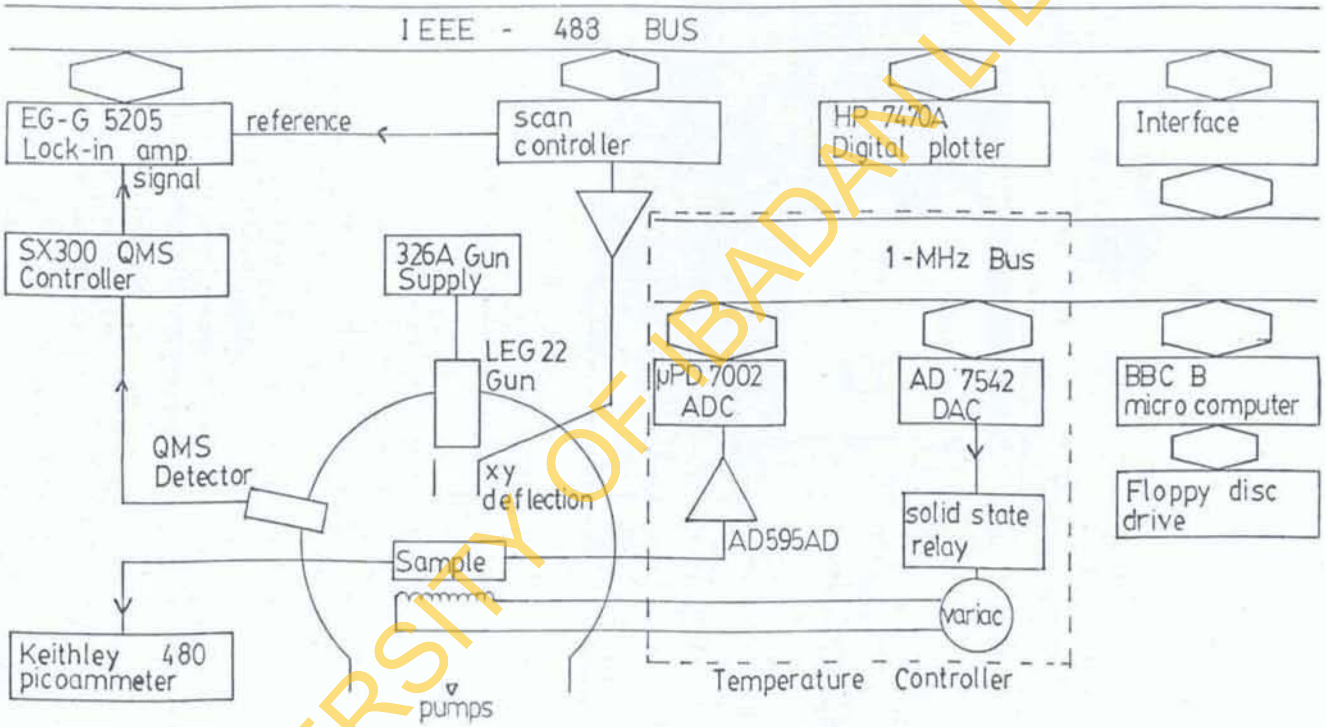

IEEE - 488 BUS
EG-G 5205 Lock-in amp
reference
scan controller
HP 7470A Digital plotter
Interface
signal
SX300 QMS Controller
326A Gun Supply
1-MHz Bus
LEG 22 Gun
μPD 7002 ADC
AD 7542 DAC
BBC B micro computer
QMS Detector
xy deflection
Floppy disc drive
solid state relay
AD595AD
Sample
variac
Keithley 480 picoammeter
pumps
Temperature Controller

Fig. 4:
Schematic diagram of the e-beam decomposition set-up

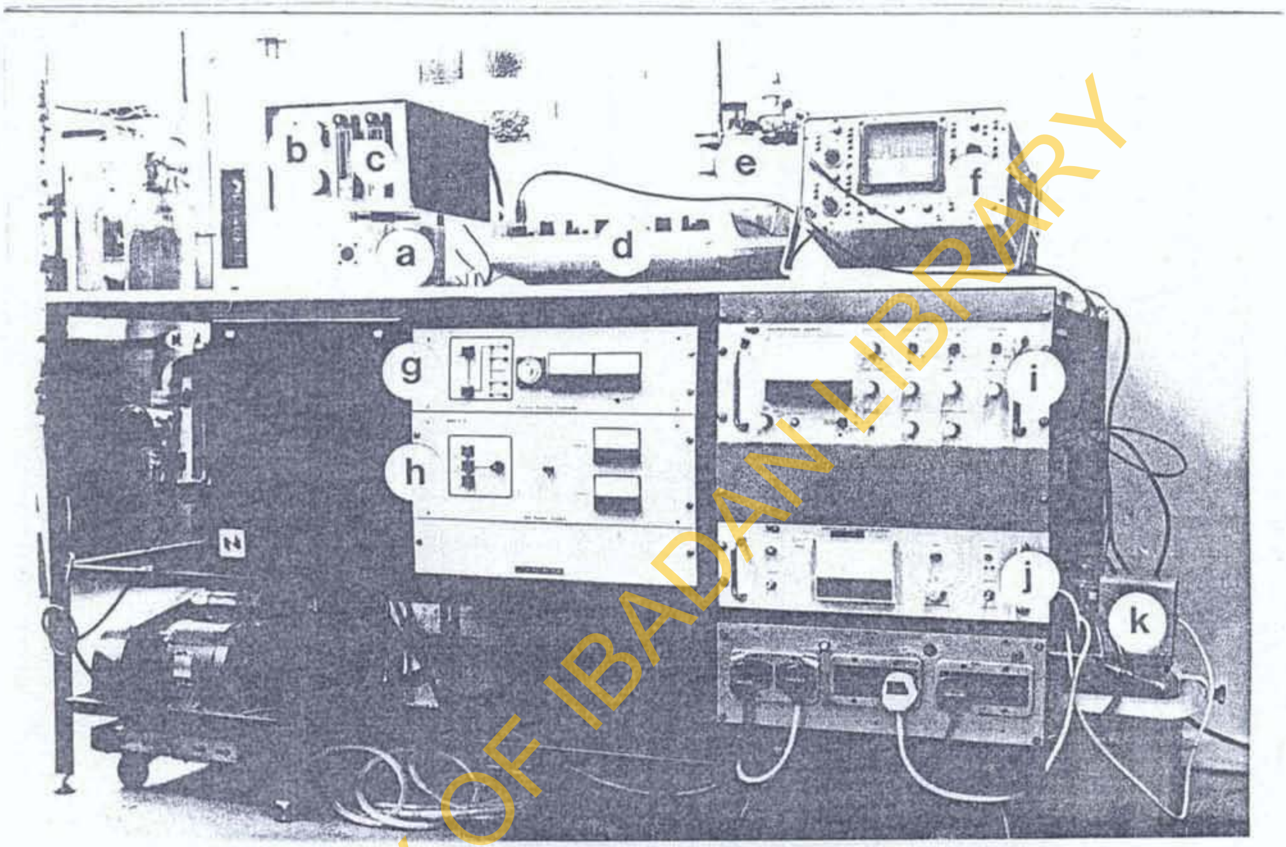


Fig. 5: Plasma and Reactive-Ion Etching Apparatus

(a) Processing chamber
(b) r.f. power matching unit
(c) Gas flow meter
(d) Y-t plotter
(e) Etch-gas supply cylinder
(f) Oscilloscope for signal monitoring
(g) Process controller
(h) r.f. power supply
(i) Micromass QX 200 QMS controller
(j) Ion pump power supply
(k) "Thermo-stirrer" for controlling the temperature of the circulating water passed through the electrodes

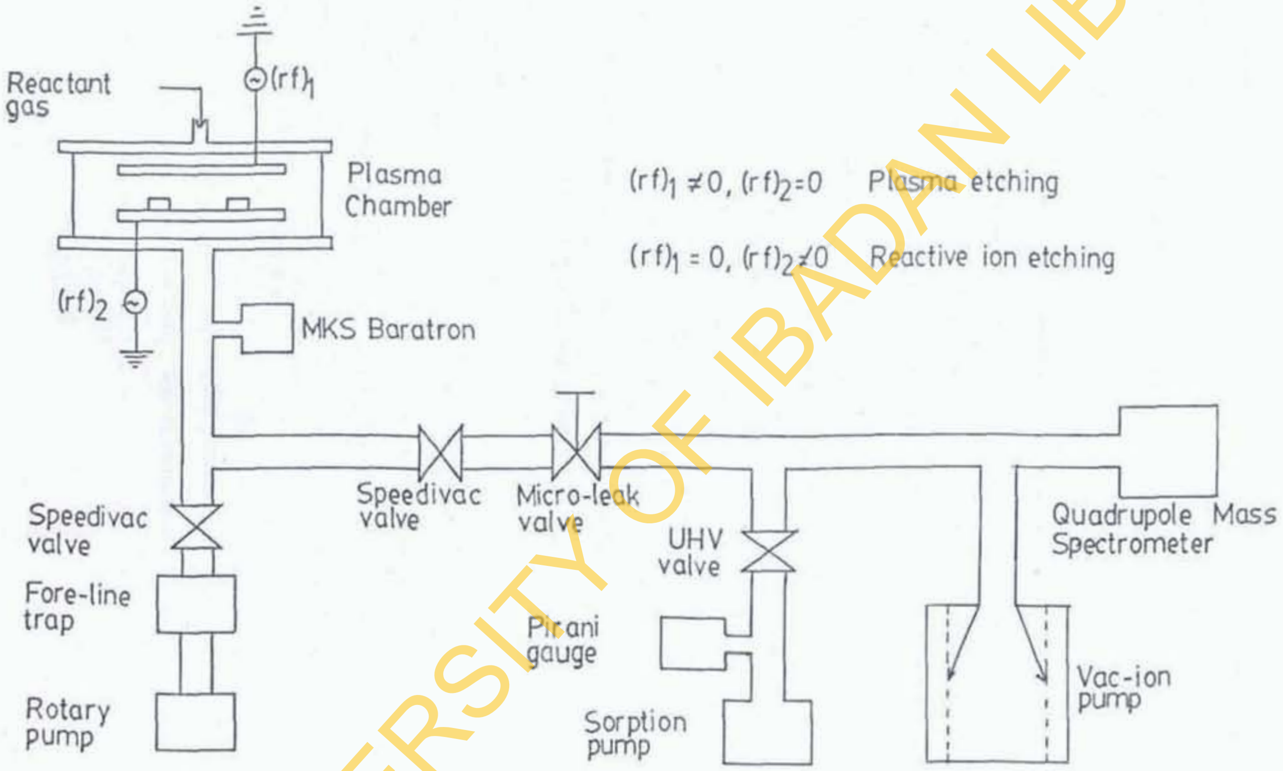

Reactant gas
(rf)$_1$
Plasma Chamber
(rf)$_1$ ≠ 0, (rf)$_2$ = 0   Plasma etching
(rf)$_1$ = 0, (rf)$_2$ ≠ 0   Reactive ion etching
(rf)$_2$
MKS Baratron
Speedivac valve
Micro-leak valve
Speedivac valve
UHV valve
Quadrupole Mass Spectrometer
Fore-line trap
Pirani gauge
Vac-ion pump
Rotary pump
Sorption pump

Fig. 6:

Schematic diagram of the plasma-assisted etching apparatus, showing a quadrupole mass spectrometer attachment.

Carbon tetrafluoride (CF_4) was the main etching gas used. In the plasma mode, oxygen (O_2) was added to CF_4 in order to prevent surface polymerisation on the $CdCl_2$ resist during etching.

To measure etch rates, film thickness was measured prior to introducing the specimen to plasma conditions, and also after the completion of etching. The change in thickness is divided by the etch time to give an average etch rate. Film thickness measurements were by ellipsometry.

End-point determination was carried out in the RIE mode. Plasma etching was abandoned because of the inadequacy of the etching. Thus it was found there was polymerisation of the resist surface, poor etch rates of SiO_2 were obtained, as well as poor selectivity in etching SiO_2 and $CdCl_2$ when CF_4/O_2 etch-gas was used.

Compositional analyses of samples were carried out by means of electron probe micro-analysis (EPMA), electron spectroscopy for chemical analysis (ESCA), and secondary ion mass spectroscopy (SIMS). Surface of samples was examined using the scanning electron microscope.

A linear relationship exists (for each of the sample SiO_2 and $CdCl_2$) between the etch rate ratios and radial distances measured from the electrode centre, due to the non-uniformity in the etch gas distribution over the wafer surface.

Preparation of samples for EPMA and surface morphology studies was carried out by mounting specimen of required size onto a 1 cm diameter brass or aluminium stub, using an electrically conducting silver paint. The sample was then gold coated for surface morphology studies, and carbon coated for EPMA. A film coating of about 10nm was found to be adequate for both studies. Compositional analyses by ESCA and SIMS were done without coating the samples.

The samples were examined in JSM-T100 scanning electron microscope, operating at 25kV, and have a resolution of 8nm. The examination was done with electron beam at an angle of 45° to the samples.

Section II: Teaching and Administrative Experience in University of Ibadan (1988 to date)

I have taught several courses at undergraduate level, which include the following:

- Network Analysis
- Electrical Machines
- Power Systems
- Power Electronics
- Electronic Circuits Design
- Operational Amplifiers & Linear ICs
- Semiconductor Devices
- Mini/Micro Computers: Hardware, Software & Applications
- Digital Systems Design
- Digital Data Transmission & Reception

In addition to my teaching assignment, I have supervised several students' projects and also held various positions of responsibilities, notably the Acting Head of the Department of Electrical & Electronic Engineering, University of Ibadan (1/12/92 to 30/9/95; 1/10/97 to date). As Acting Head of Department, I am responsible to the University Senate:

- for the teaching and the general administration of the Department,
- for the organization and control of courses of study and examinations in the department
- for the choice and assignment of final year project titles to final year students in the department.

In discharging my duties, several modules have been designed and constructed for use in the laboratories. This is to cope with the shortage of laboratory equipment, due to lack of funds. Reports of some of the modules constructed as Appendices I - III.

Section III: Teaching and Administrative Experience outside University of Ibadan (1988 to date)

I have taught and performed some administrative duties at Lagos State University (LASU), as Associate lecturer (January 1990 to August 1995) and during my sabbatical period ([illegible] 199[illegible] to [illegible] 19[illegible]7). During these periods, I have taught several courses, similar to those listed in Section III, and supervised several students' projects.

During my sabbatical period at LASU, I held the following positions of responsibilities and performed various tasks, such as:

- Acting head of the Department of Electronics & Computer Engineering
- Member of the Programme Implementation Committee for the UNDP-Assisted Project
- Spearheaded the development of a new curriculum for the department, under the UNDP-Assisted Project
- Considerable experience in the use of Computer packages
- Involved in the Networking of the Computer laboratory - Bus topology for 50 PCs
- Delivered series of lectures at several courses organised on "Word Processing & Desktop Publishing"
- Course Coordinator for several "Continuing Engineering Education Programmes (External courses for practicing engineers, such as 'Electronic Equipment: Its Application & Maintenance,' and 'PC Maintenance'."

Section IV: Major conferences/Workshops attended

Major Conferences/workshops attended since 1988 include:

- 4-day critique workshop on the revised curriculum for the undergraduate programme in Electronic & Computer Engineering held at ASCON, Topo Badagary (2-5 September, 1996)
- Workshop Seminar on Installation of Novell Network in LASU UNDP-Assisted Laboratory (29th July - 2nd August, 1996)
- 1st National Conference on the Role of Practitioners of Instrumentation & Control Engineering in National Technological Development, 19-20 September, 1991, University of Ibadan Conference Centre.
- Experimental Workshop on High Temperature Semiconductors & Related Materials (Basic Activities) 12-30 March, 1990, Trieste, Italy.

APPENDIX I

A DIGITAL CAPACITANCE METER

1. INTRODUCTION:

It is a fact that most university laboratories and some electronic workshops in the country cannot boast of an instrument that can measure, accurately, the value of one of the fundamental components in electronics and electrical engineering - the capacitor.

A capacitor is simply a component that can store electric charge.

The capacitor can be required in a number of applications: such as in isolation of dc biasing and coupling of various stages in a multistage amplifier; filtering out an unwanted frequency component; storage of voltage level for a defined period (e.g., Sample and Hold circuit in communication circuits); shaping the frequency response of an operational amplifier; and removing ripples from a power supply.

In all these applications, the capacitance (value of the capacitor) has to be specified. The capacitance C, of a parallel plate capacitor is defined as:

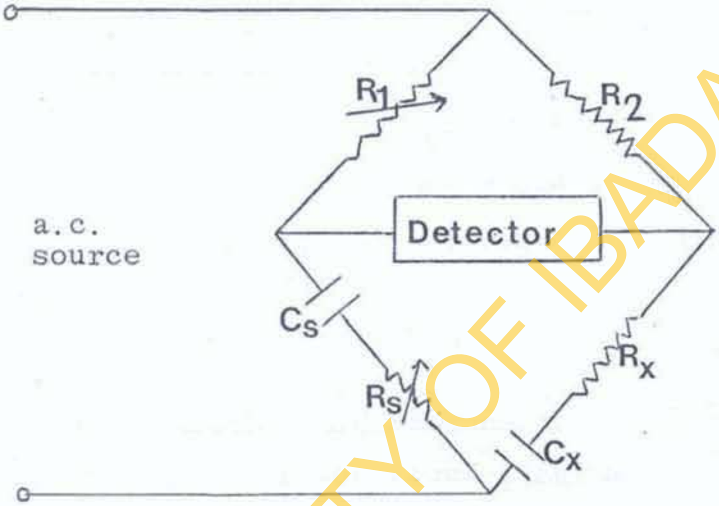
$$C = \frac{\epsilon_o \epsilon_r A}{d}, \quad \text{Farads} \text{ --- } (1)$$

where ϵ_o is permitivity of free space in F/m, ϵ_r is dielectric constant, A is the cross-sectional area of the plates in m^2 and d is the separation distance of the plates, in m.

Capacitors are usually classified by the dielectric material (ϵ_r in Eqn.1). The dielectric material is an insulating medium and some examples are polyester, polysterene for high voltages, ceramic for small capacitances, air or thin mica sheets for variable capacitors. Thus for a given dielectric material, the capacitance of the capacitor depends on parameters A and d.

1.1 Bridge Method of Capacitance Measurement

The most common way of measuring capacitance is the alternating current (ac) bridge method, Fig. 1.



a.c.
source

Cs and Rs are
standard values

Rx and Cx are unknown.

Fig. 1: A capacitance comparison bridge circuit.

The balance equation of the ac bridge is given by the equation,

$$R_1(Rx - \frac{j}{wc_x}) = R_2(Rs - \frac{j}{wcs}) \quad - \quad (2)$$

$w = 2\Pi f$, where f is the ac source frequency.

Equating separately the real and imaginary parts give the following equations:-

$$Rx = Rs \frac{R_2}{R_1} \quad — \quad (3)$$

and $$Cx = Cs \frac{R_1}{R_2} \quad — \quad (4).$$

The detector could be a pair of headphones whereby adjustment of R_1 gives a minimum sound which indicates the balance point.

The major drawback of this method is that the accuracy of measurement depends on the individual making the measurement; similar to the parallax error introduced in using analog meters. The error due to this drawback could be minimised by using a digital means for capacitance measurement.

1.2 Digital Means of Measuring Capacitance

Fig. 2 is the block diagram of a digital circuit that can be used to measure capacitances. The test capacitor which is the capacitance to be measured, is part of an R-C timing network. The timing circuit network form part of a monostable multivibrator and the higher the value of the test component the longer the output pulse of this circuit.

A low frequency oscillator (LF. Osc.) controls the rate at which readings are taken, and this gives readings at just under one second intervals. Its output drives a simple control logic circuit, the output pulses of this circuit sequences the rest of the circuit.

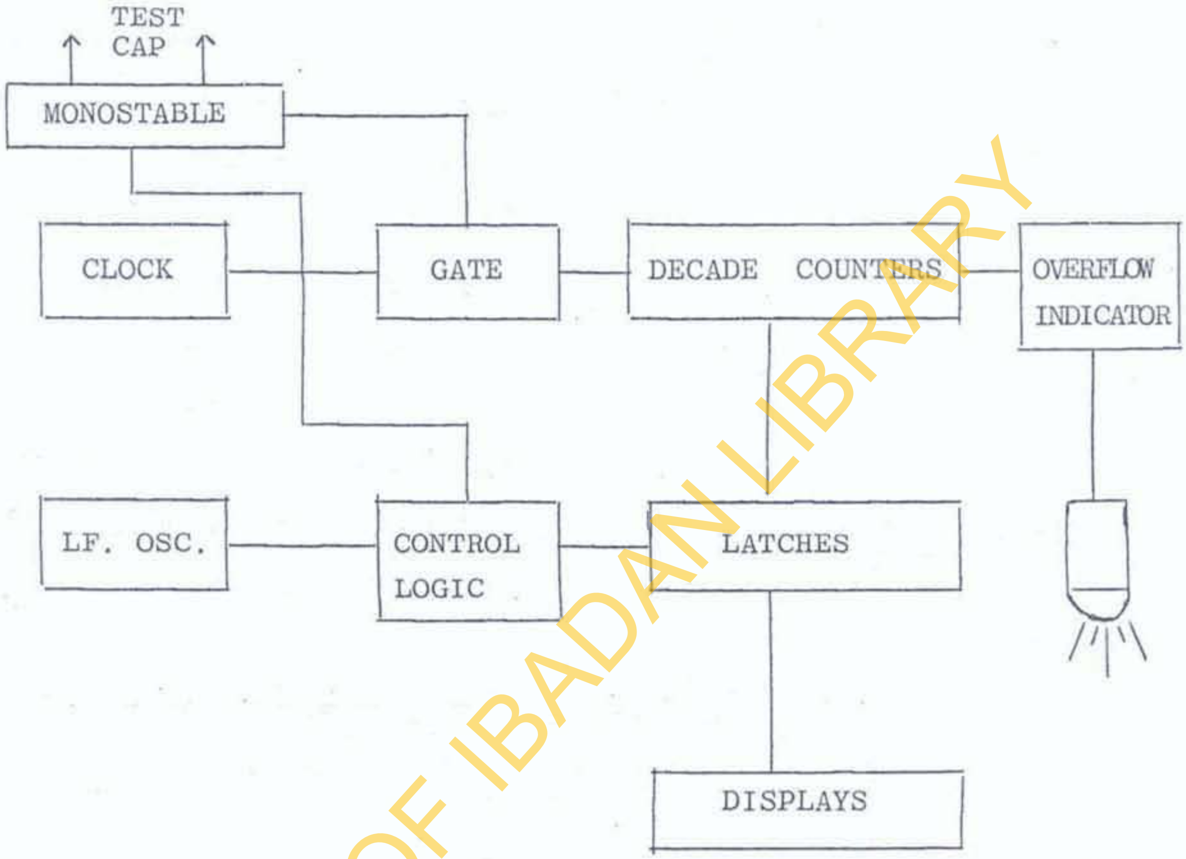

TEST
CAP
MONOSTABLE
CLOCK
GATE
DECADE COUNTERS
OVERFLOW INDICATOR
LF. OSC.
CONTROL LOGIC
LATCHES
DISPLAYS

Fig. 2: Block Diagram of the Capacitance Meter.

The first pulse (trigger pulse) is applied to the monostable multivibrator whose output pulse, which depends on the test capacitor, is needed as a gate pulse to count the pulses coming from the clock oscillator. At the end of the gate pulse (the one-shot pulse produced by the monostable multivibrator), the count is frozen. The latch pulse from the control logic circuit enables value of the test component to be displayed. The overflow indicator is an indication that the value of the capacitor is beyond the range selected.

2. THE DESIGN:

The major circuits, as shown in Fig. 2, are:

(i) The Low Frequency oscillator;

(ii) The control logic;

(iii) The monostable multivibrator;

(iv) The clock/counter; and

(v) The overflow indicator.

The CMOS logic ICs are used in the design. It has been chosen in preference to the TTL because speed is of no importance in the capacitance meter and moreover, its other features make it desirable in this design.

2.1 The Low Frequency Oscillator Circuit.

This is an astable multivibrator circuit as shown in Fig. 3.

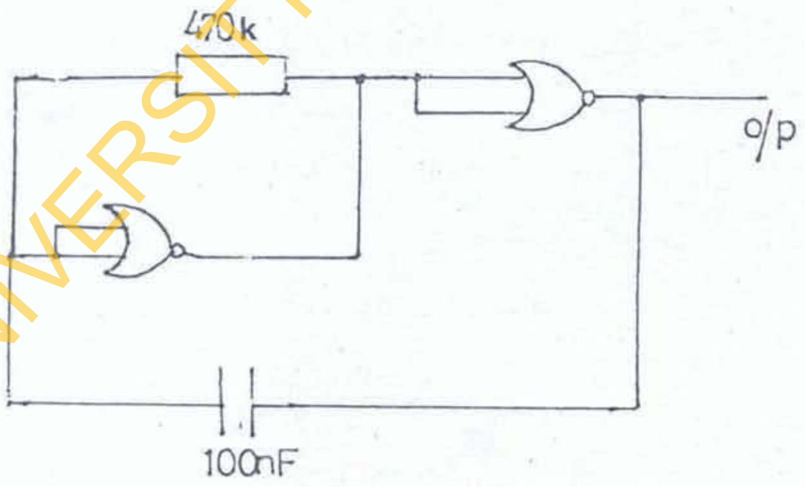


Fig. 3: Low Frequency Oscillator.

This oscillator has to be of a higher frequency than the other circuits so as to give readings under one second interval. The 'on' and 'off' times are controlled independently by forcing the capacitor to charge and discharge through a resistor.

The time duration of a single pulse is given by,

$$T = 0.693\ RC$$

for $R = 470K\Omega$ and $C = 100nf$

$$T = 0.693 \times 470 \times 10^{3} \times 100 \times 10^{-9}$$

$$= 0.03257 \text{ seconds.}$$

Time for ten output pulses needed to complete one measurement cycle, is 0.32571 seconds, still far less than one second.

2.2 Control Logic Circuit

The CMOS 4017 BE was chosen. It has ten separate outputs offering a completely decoded count, each output pulse sequentially repeating every 10 counts. The control logic circuit is shown in Fig. 4. Out of the ten pulses produced, pulse '0' is for reset, pulse '1' for trigger and pulse '9' for latch. The remaining '2 to 8' pulses are to provide time for the duration of the gate pulse.

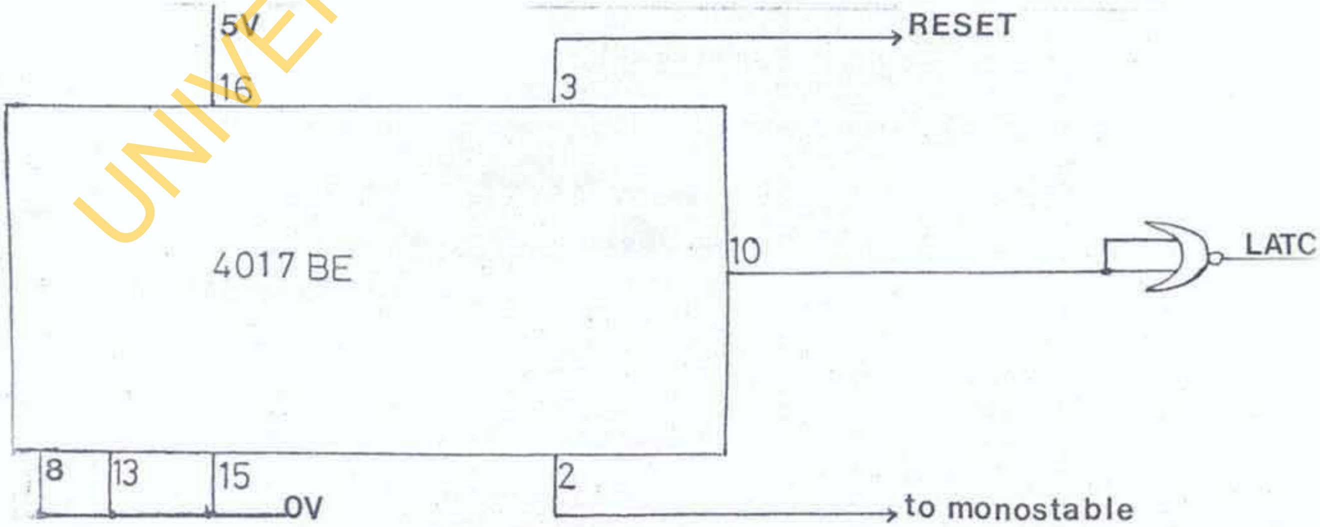


Fig. 4: Control Logic Circuit.

2.3 Monostable Circuit

The circuit (Fig. 5) is made up of two NOR gates, the test capacitor and the range resistor.

A non-retriggerable monostable multivibrator is employed so that if the trigger pulse duration from one of the NOR gates is longer than the duration of the output pulse there would be no effect on the display reading.

The range resistors (six in all) each have a tolerance of 1% which allows for maximum accuracy and avoidance of callibrating, individually, each range which would be rather cumbersome. By reducing the timing resistance (range resistors 10M-100ohm) in decade steps, the timing capacitor (10nf to 1000μF) needed for a reading is boosted in decade increment.

2.4 Clock Oscillatory Circuit

The NE 555V timer is employed as a free-running multivibrator (Fig. 6).

This mode of operation is for the continuous generation of pulses whilst the gate pulse from the monostable is available.

The on time, $t_{on} = 0.693(R_1+R_2)C$, also

The 'off' time, $t_{off} = 0.693R_2C$.

For this design, t_{on} and t_{off} are determined by the variable resistor. The variable resistor is used for calibration to enable the right amount of pulses to be sent to the counter circuit.

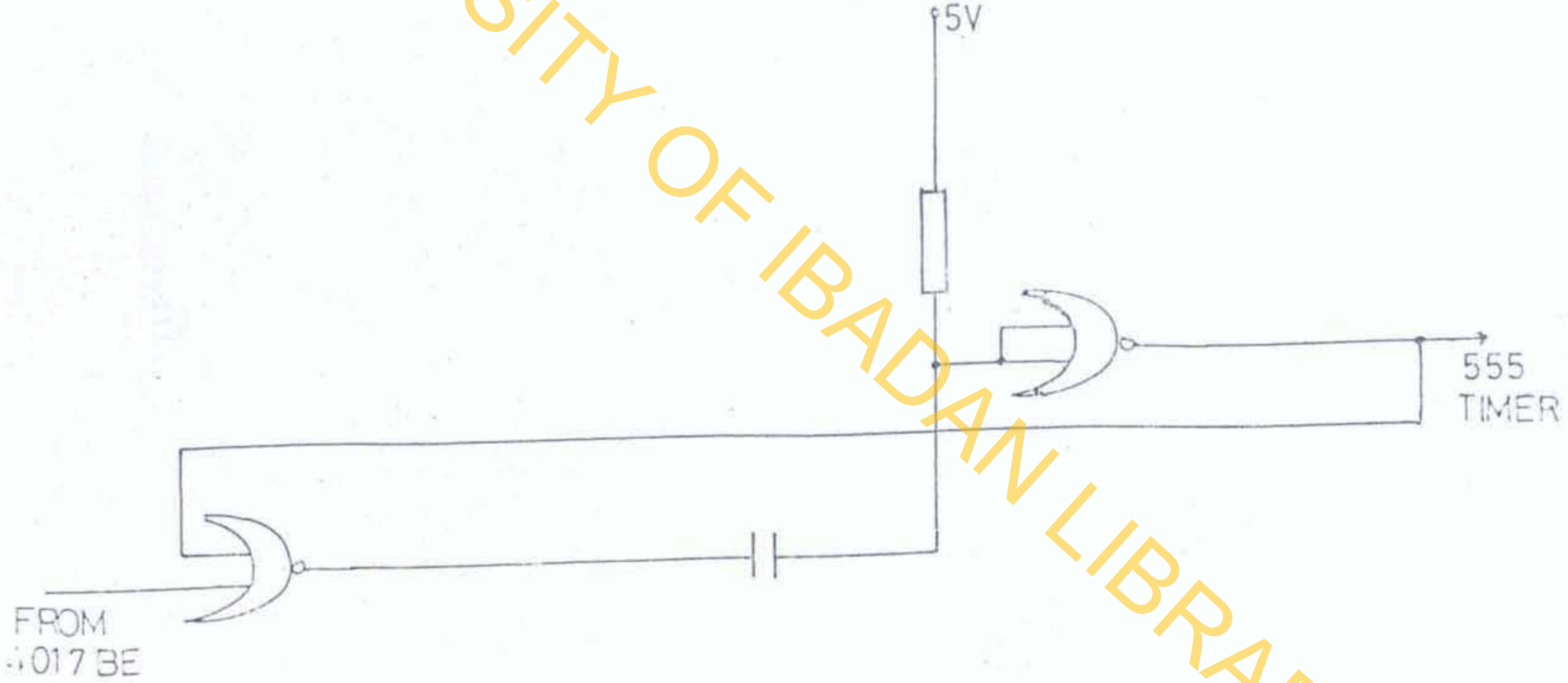

5V
555
TIMER
FROM
4017BE

Fig. 5: Monostable Circuit.

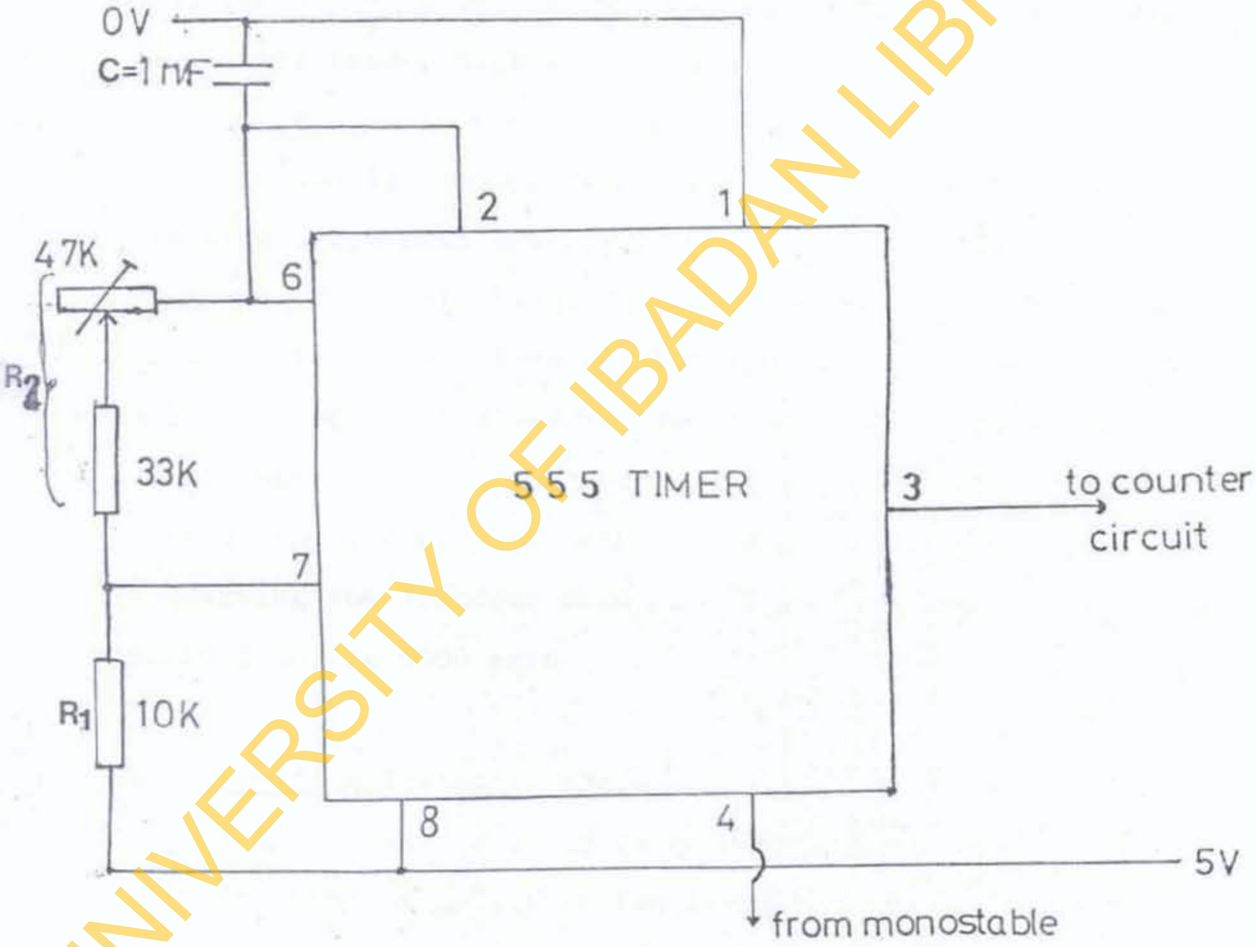

0V
C=1 nF
2
1
47K
6
R2
33K
555 TIMER
3
to counter circuit
7
R1
10K
8
4
5V
from monostable

Fig. 6: Clock oscillatory circuit.

2.5 Counter Circuit

The counter circuit (Fig. 7) counts the pulses from the clock oscillatory circuit. The reading is displayed when the last pulse (latch pulse) from the control logic circuit has been received by the counter circuit.

The IC 40110BE counter, can only drive common cathode displays. The current flow from the counter to the display is usually rather high as a result, resistors are used as an interface between both components.

The display, which is 0.5 inches, is chosen because of its high brightness featuring highly legible, bold, solid segments, fast switching, low power comsumption and compatibility with ICs. When all the four segments are on display, a current of about 100mA may be drawn from the power supply, so six batteries of 1.5V each are used. The reset from the control logic circuit resets the counter, although not disturbing the 'frozen' count so as to have the next reading start from its 0000 mark.

2.6 Overflow Indicator Circuit

This circuit (Fig. 8) is to enable the users realize that the test capacitor is too large for the range chosen.

A CMOS IC 4013BE, which is a dual - D type Flip-Flop, and two NOR gates CMOS IC 4001BE are used.

2.7 The Module

Figs. 9 and 10 combined, are the whole circuitry. The whole circuit is enclosed in an enclosure of 205 x 140 x $40mm^3$,

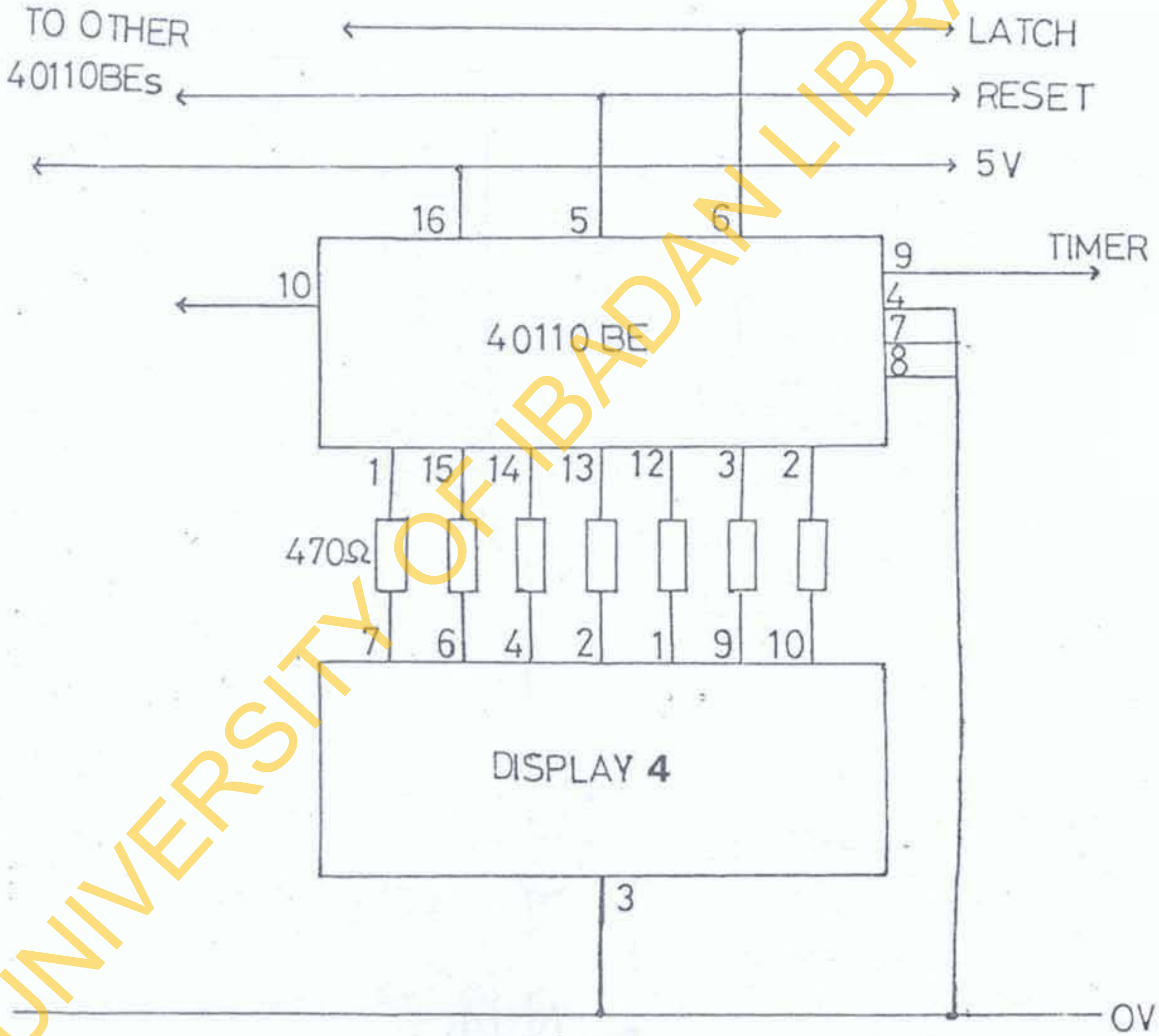

TO OTHER
40110BEs
LATCH
RESET
5V
16
5
6
TIMER
9
4
7
8
10
40110 BE
1
15
14
13
12
3
2
470Ω
7
6
4
2
1
9
10
DISPLAY 4
3
OV

Fig. 7: Typical counter circuit.

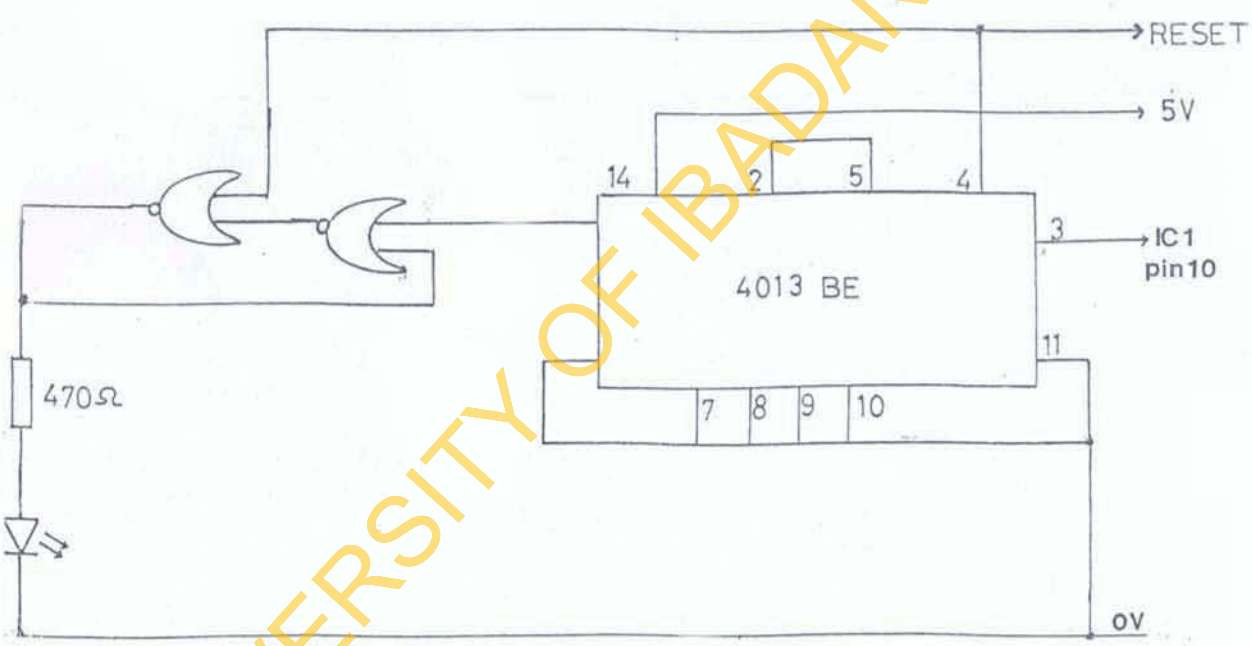
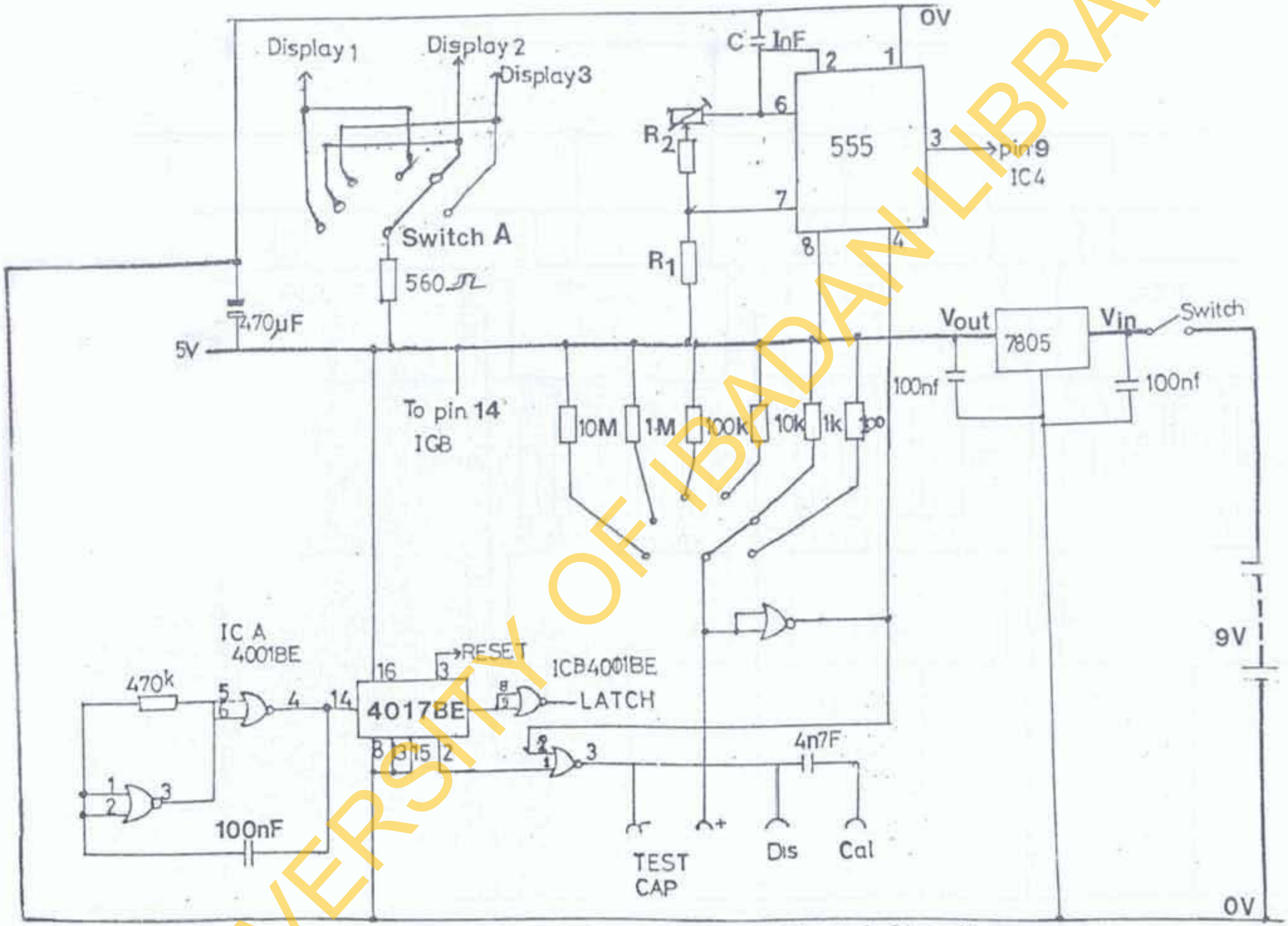

RESET
5V
14
2
5
4
3
IC1
pin10
4013 BE
11
7
8
9
10
470Ω
0V

Fig. 8: Overflow indicator circuit.



0V
Display 1
Display 2
Display 3
C
1nF
2
1
6
R2
555
3
pin 9
IC4
7
Switch A
R1
8
4
560Ω
470μF
5V
Vout
7805
Vin
Switch
100nf
100nf
To pin 14
ICB
10M
1M
100k
10k
1k
100
IC A
4001BE
RESET
ICB4001BE
LATCH
470k
5
6
4
14
16
3
4017BE
8
9
8
13
15
2
2
1
3
4n7F
1
2
3
100nF
TEST
CAP
+
Dis
Cal
9V
0V

Fig. 9: Part 1 of the Digital Circuit.

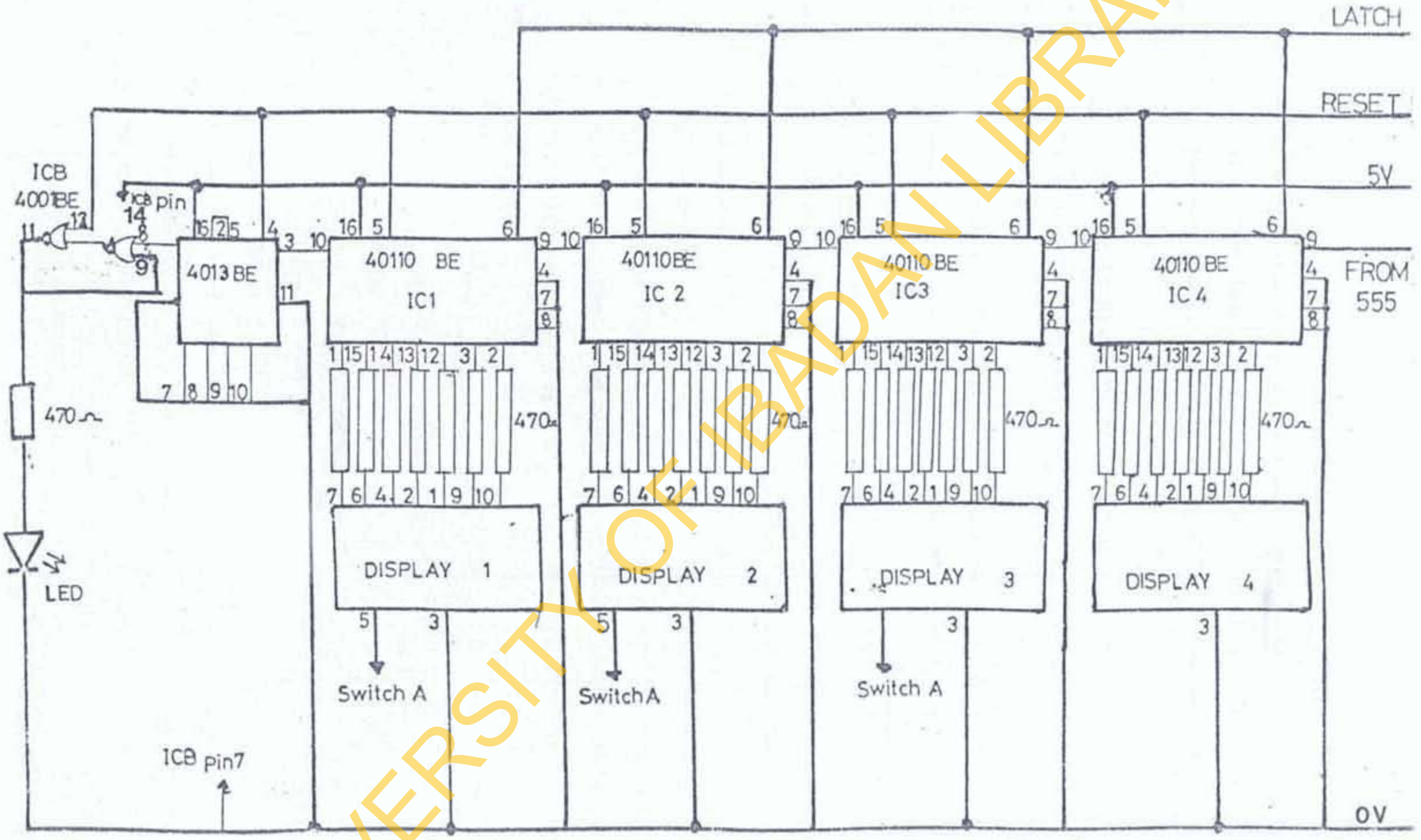

LATCH
RESET
5V
FROM 555
0V
ICB 4001BE
ICB pin 14
4013 BE
40110 BE IC1
40110BE IC 2
40110 BE IC3
40110 BE IC 4
470Ω
DISPLAY 1
DISPLAY 2
DISPLAY 3
DISPLAY 4
Switch A
Switch A
Switch A
LED
470Ω
ICB pin7

Fig. 10: Part II of the Digital Circuit.

made of plastic (top and bottom), and metal (front and back) panels. The display window is cut out on the left handside of the top panel, installed with an LED display filter which is anti-glare.

In the front panel are four sockets, 6 way-2 pole rotary switch, overflow indicator and an ultra-minimum toggle switch.

The unit has an in-built calibration capacitor to check the validity of any reading being obtained.

3. CONCLUSION:

A digital capacitance meter capable of measuring capacitances in the range of 1nF to 1000µF has been designed and constructed. The meter is powered by an internal 9 volt battery, and is consequently fully portable. An overflow indicator circuit is also included to show when the value of the test component is out of the chosen range. The design has four digit LED display covering the following six ranges:

Range 1, 0 to 9.99nF
Range 2, 0 to 99.99nF
Range 3, 0 to 999.9nF
Range 4, 0 to 9.99µF
Range 5, 0 to 99.9µF
Range 6, 0 to 999.9µF

The accuracy of the meter was found to be quite good giving typical error of ±2% in measurements. The device is now in use in our department.

The project is cheap and all components used are available in the country. Parallax error is eliminated.

APPENDIX II

A UNIQUE POWER SUPPLY UNIT WITH AN APPROPRIATE TRANSFORMER

1. INTRODUCTION

One of the most basic and necessary systems, or more specifically subsystems, in electronics is the direct current (dc) power supply. In communication equipment, instrumentation, computers, or any electromechanical systems, small or relatively large, a source of dc power which is furnished by a dc power supply is required.

Basically, the function of a dc power supply is to convert the readily available 230V, 50Hz alternating current (ac) voltage into a well regulated, fixed or variable, dc voltage. The power supply, therefore, must contain the following circuits:

(1) the transformer, which either steps up or steps down the available ac voltage to the required level;

(2) the rectifier circuit, which converts the ac voltage into unidirectional or pulsating dc voltage;

(3) a filter circuit, which removes or minimizes the ripple; and

(4) a regulating circuit, which maintains the dc voltage level at the required output value irrespective of variation in either the load or the input ac supply voltage.

The scope of the design is to meet the following specifications: ±5V,IA; ±12V,1A; 0-40V,1.5A; and 0-(-34)V,1.5A.

To meet these specifications, an off the shelf transformer cannot be used, therefore, an appropriate transformer has to be designed and constructed to achieve the dc power supplies requirements. Thus, this work has its basis on a good transformer design.

2. TRANSFORMER DESIGN.

2.1 Transformer Classifications

Transformers are used to meet a wide range of requirements. Poly-type distribution transformers supply relatively small amount of power to residential houses. Power transformers, depending on the size, are employed: (i) at generating stations to step up the generated voltage to high level of transmission to minimize losses; (ii) at substations to step down the transmitted voltages for local distribution; and (iii) in electronic circuits power supply unit, to step down the available ac voltages. Instrument transformers are used to measure voltages and currents. Audio and video transformers must function over a broadband of frequency. Radio frequency transofrmers transfer energy in narrow frequency bands from one circuit to another. A power transformer designed to meet the requirements of electronic circuits, is to be implemented.

2.2 The Design

In transformer design, most of the basic design principle are applicable to all the aforementioned transformers, but attention will now be focused on the design of the power transformer. The power transformer required for the above specifications is a 240V/8A primary winding and multi-windings secondary having centre-tapped values of 32V, 28V, 24V and 18V. The number of turns of wire for both primary and secondary windings are obtained from the transformer designers' equation [1-5] ;

$$\frac{N}{E} = \frac{10^8}{4.44B_{max}Af} \qquad \text{——} \qquad (1)$$

where N is number of turns of wire to induce the emf voltage E, B_{max} is the maximum flux density to prevent magnetic core saturation, A is the crosss-sectional area of the insulating former (Fig. 1) of the transformer and f the operating frequency.

Fig. 1 shows thecomplete transformer core assembly.

In choosing the core material from the listings in Table 1 [6], the silicon content of iron and nature of annealing are very important in that they have a direct bearing on the hysteresis loss. The first three are

TABLE 1[6]: TRANSFORMER CORE MATERIALS AND THEIR CHARACTERISTICS

MATERIAL	ρ	$\mu_o$dc	μ_{max} dc	(B-H) Gaus	Sat. Lines/ sq. in
Mumetal	62	30,000	130,000	5,500	55,000
Permalloy C	60	16,000	7,500	5,000	52,000
Radiometal	55	2,200	22,000	16,000	103,000
Permalloy B	45	2,000	15,000	11,000	103,000
Permalloy A	20	12,000	90,000	8,000	71,000
Cr-Permalloy	65	12,000	60,000	8,500	52,000
Mo-Permalloy	55	20,000	75,000	6,000	55,000
1040	56	40,000	100,000	9,300	39,000
Megaperm	97	3,300	68,000	15,500	60,000
Hipermck	46	3,000	70,000	16,000	100,000
45 Permalloy	45	2,700	23,000	12,000	103,000
Rhometal	95	250-2000	1200-8500	19500	125000
4% Silicon Steel	55	450	8000	16000	125000

ρ = resistivity in microhm cm; μ_{odc} = initial permeability

$\mu_{max}{}^{dc}$ = maximum permeability obtainable

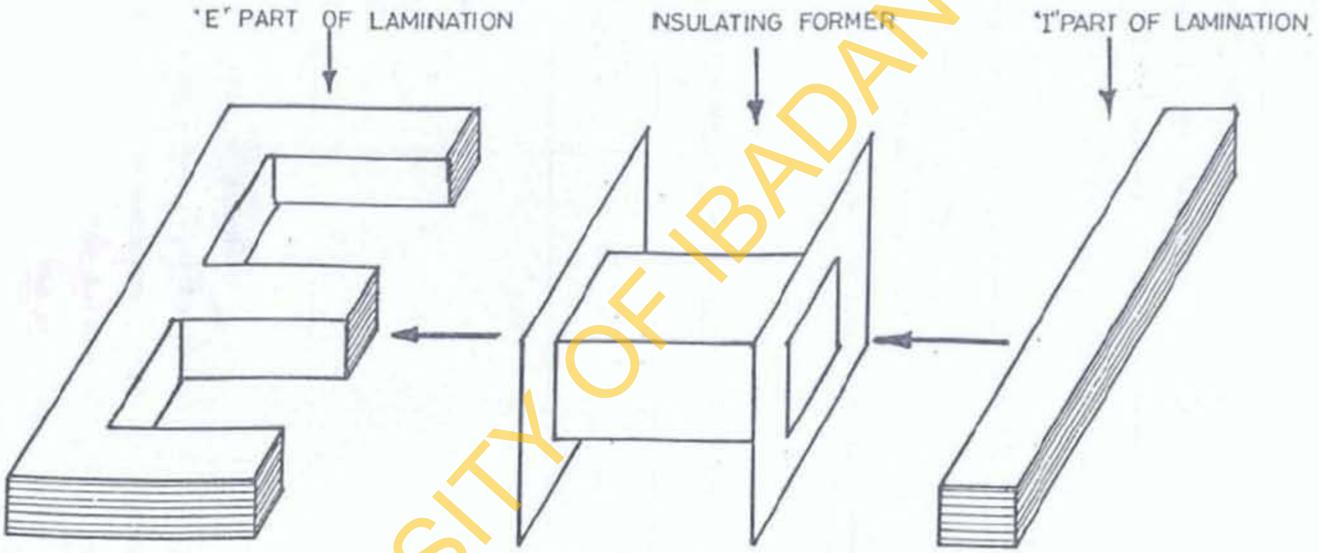

'E' PART OF LAMINATION
INSULATING FORMER
'I' PART OF LAMINATION

Fig. 1: Transformer Core Assembly.

materials are the most commonly used for low voltage, single phase transformers [6]. The permalloy C was chosen for this work, and to prevent magnetic saturation, B_{max} value of 50,000 lines/in^2 was used. With a cross-sectional area of the core of 2.74 in^2 (1.68in x 1.62in), then number of turns/volt equals 3.29.

In the practical implementation, the number of turns of wire per volt of 4 resulted in total number of primary winding of 880 turns for a 220V ac supply. The number of turns for various secondary voltages are listed in Table 2.

TABLE 2: SECONDARY VOLTAGES AND CORRESPONDING WINDING TURNS

Secondary voltages (V)	Secondary Winding turns	Power Supply voltages (V)
32	128	0-40
28	112	0-(-37)
24	96	±12
18	72	± 5

Enamel cable of standard wire gauges (s.w.g) 22 and 24 were used to meet the required specifications for the primary and secondary windings, respectively. The disparity in the s.w.g. is due to the followings: available winding area; and highercurrent in the secondary circuit (since the same power is transformed from the primary circuit to the secondary circuit, then stepping down the voltage will result in higher current in the secondary circuit).

Most transformers are wound by winding machine which makes the job quite fast, neat and ensures accurate number of turns. Due to either non-availability or non-functionality (when found) of such machine, the winding was done manually. It has to be mentioned that manual winding is very tedious, and requires absolute concentration as well as greater care to avoid making any mistake. The winding process commenced in the clockwise direction until half the required number of turns had been wound. Since the enamel cable is coated, insulation at this point of half total number of turns was removed, and a wire tapping soldered to the point. This serves as the centre-tap point and the winding process continued in the same direction until the required number of turns had been wound, with the end point brought out. The whole coil was insulated properly using paper tape, this being in addition to the insulation offered by the coating of the wire. Secondary windings were also done and insulated accordingly.

Appropriate measurements, such as the continuity test, efficiency, regulation, heat resistance test, indicated that the final design and constructed transformer is in accordance, within allowable experimental error, with the original aim of the design.

3. SIGNAL CONDITIONING CIRCUITS

The signal conditioning circuits comprise of the following: rectifying, filter, and the regulating circuits.

3.1 Rectifying Circuit

Rectifiers are used primarily for the conversion of ac voltages to dc voltages. In semiconductor technology, the device that meets this definition is known as a pn junction diode. It is a component that allows current to flow in one direction but blocks the flow of current in the other direction.

There are various rectifying circuits; such as the half-wave and full-wave rectifying circuits.

3.1.1 Half-wave Rectification

A half-wave rectifying circuit is shown in Fig. 2, with the appropriate input and output waveforms. This type of circuit is practicable only for light load condition so that the transformer core does not reach dc saturation.

3.1.2 Full-wave Rectifier Circuit

Full-wave rectifier circuits are as in Figs. 3a and b. In the circuit of Fig. 3a, each diode voltage rating is twice the peak reverse voltage, also a centre-tapped transformer having twice the overall voltage rating is employed. These are serious drawbacks. To overcome these drawbacks, the circuit of Fig. 3b, which is a bridge rectifier circuit, is employed. Bridge rectifier circuits are useful in both single-phase and poly-phase applications.

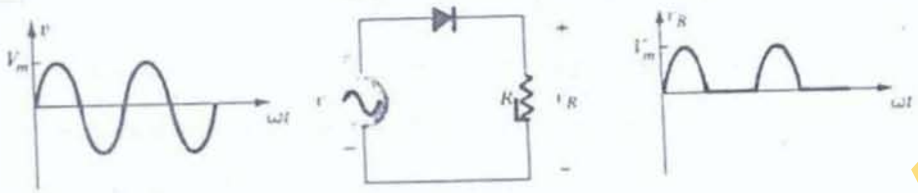

v
V_m
ωt
+
v
−
R
v_R
+
−
v_R
V_m
ωt

Fig. 2: Half-wave Rectification.

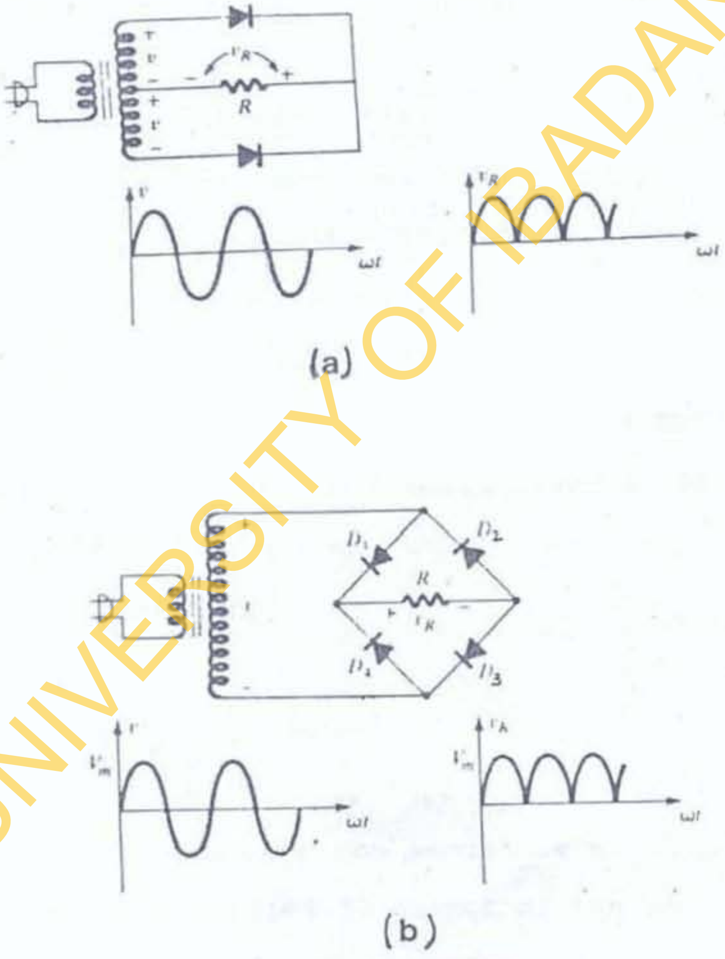

+
v
−
+
v
−
v_R
−
+
R
v
ωt
v_R
ωt
(a)
D_1
D_2
R
+
v_R
−
D_4
D_3
v
V_m
ωt
v_R
V_m
ωt
(b)

Fig. 3: Full-wave Rectification.

3.1.3 Characteristics of Rectifiers

3.1.3.1 Peak Inverse (or Reverse) Voltage (PIV)

This is the voltage that the diode rectifier must withstand when it is non-conducting. For a well-designed power supply, the maximum value of the inverse voltage should not exceed the rated value of the rectifier specified by themanufacturer. It is then obvious that this PIV is shared by two diodes in the bridge rectifier circuit of Fig. 3b, while a single diode has to withstand this amount of voltage in the circuit of Fig. 3a.

3.1.3.2 Current Ratings

Another important rating for a rectifier is the average current through it. The average rectifier current of a half-wave single-phase rectifier is the same as the average load current. For a full-wave single-phase rectifier, the average rectifier current is one-half the average load current. The maximum value of instantaneous current through the rectifier should not exceed the peak current rating of the rectifier.

3.1.4 Ripple Factor

The term 'ripple factor' (illustrated in Fig. 4) is used to evaluate the amount of ac component still present in the rectified dc output of the rectifier. Ripple factor, r, is given by the equation,

$$r = \frac{\text{rms value of ac component}}{\text{dc value of output signal}} \quad \text{—— (2).}$$

The ripple factors for half-wave and full-wave rectifier circuits are 121% and 48% respectively.

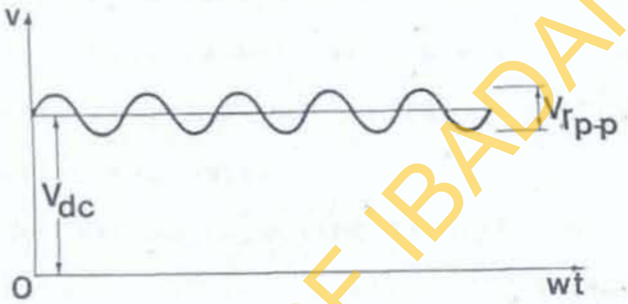
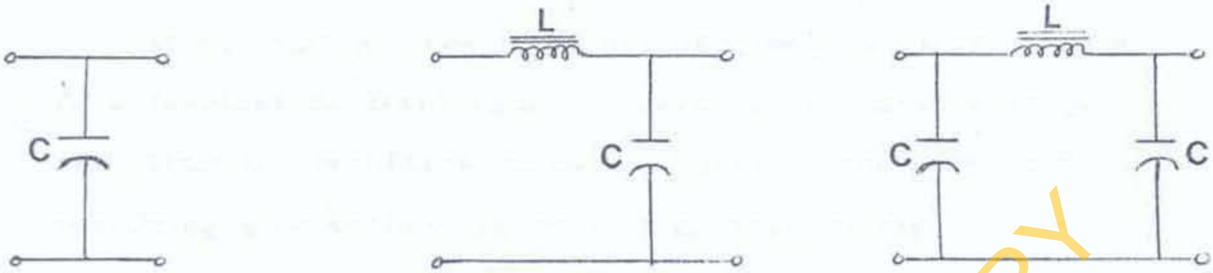


Fig. 4: Filter voltage waveform showing dc and ripple voltages.

3.2 Filters

Though the ripple factor of the full-wave circuit is much lower than that of the half-wave, the percentage of the ac component is still unsatisfactory for most electronic purposes. Thus, a filter circuit has to be employed to remove the unwanted ripple variation in the output voltage to produce a smooth dc supply.

There are various filter circuits (Fig. 5) such as the simple capacitor filter, the L-section filter and the pi-filter.



(a) Simple Capacitor Filter (b) L-Section Filter (c) Pi-Filter.

Fig. 5: Filter Circuits.

For the purpose of this design, the simple capacitor filter circuit is more than adequate, this is because the inductors required for low ripple are somehow bulky and relatively expensive.

The simple capacitor filter circuit of Fig. 5a, is connected across the rectifier output and the dc output voltage is available across the capacitor. Figs. 6a & b are the rectified and filtered outputs, respectively. As shown, the filtered voltage has a dc level with some ripple voltage super-imposed on it.

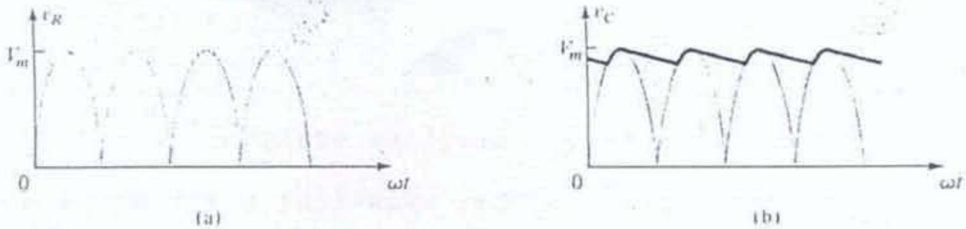


Fig. 6: Capacitor filter operation: (a) full-wave rectifier voltage; (b) filtered output voltage.

At no load ($R = \infty$), the output waveform would ideally be a constant dc level equal in value to the peak voltage (Vm) from the rectifier circuit. However, the purpose of obtaining a dc voltage is to provide this voltage for use by other electronic circuits, which then constitute a load on the voltage supply. Fig. 7 shows the output waveform of the capacitor filter circuit approximated by straight line charge and discharge

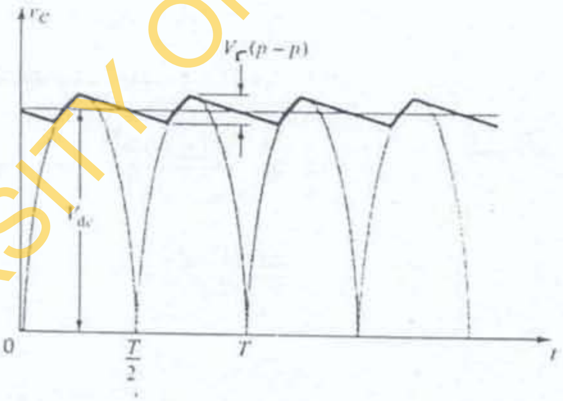


Fig. 7: Approximate output voltage of capacitor filter circuit.

By the appropriate analysis, the following relations are obtained for a full-wave rectifier and capacitor filter circuits:

$$V_{dc} = V_m - \frac{V_{rp-p}}{2} \quad — \quad (3)$$

$$\text{and} \quad V_{r(rms)} = \frac{V_{rp-p}}{2\sqrt{3}} \quad — \quad (4)$$

If Idc is the average current drawn from the filter by the load, and C the filter capacitor value, then;

$$V_{r(rms)} = \frac{Idc}{4\sqrt{3}FC} \times \frac{Vdc}{Vm} \quad — \quad (5)$$

F, being the operating frequency.

For light load, V_{dc} is only slightly less than Vm, therefore,

$$V_{r(rms)} \quad \frac{Idc}{4\sqrt{3}\,FC} \quad — \quad (6)$$

Using the definition of ripple (Eq. 2) and the equation for ripple voltage (Eq. 6), then the ripple factor of a full-wave capacitor filter is;

$$r = \frac{V_{r(rms)}}{V_{dc}} \times 100\% = \frac{Idc}{4\sqrt{3}x50xC} \times \frac{1}{V_{dc}} \times 100\%$$

$$\therefore \quad r = \frac{2.9Idc}{CV_{dc}} \times 100\% \quad — \quad (7)$$

Alternatively,

$$r = \frac{2.9}{R_L C} \times 100\% \quad — \quad (8)$$

Idc is in mA, C in microfarads, Vdc is in volts and R_L is in Kilo hms.

Thus r vary directly with the load current (high load current, high ripple factor), and inversely with the capacitor size.

3.3 Regulator Circuit

A regulator circuit maintains a rated output voltage under all conditions; either no load (open circuit) or full load (short circuit) supplying an output current. A practical regulator characteristic is shun in Fig. 8, where the output voltage under load, V_L is lower than the no-load output voltage, V_{OL}

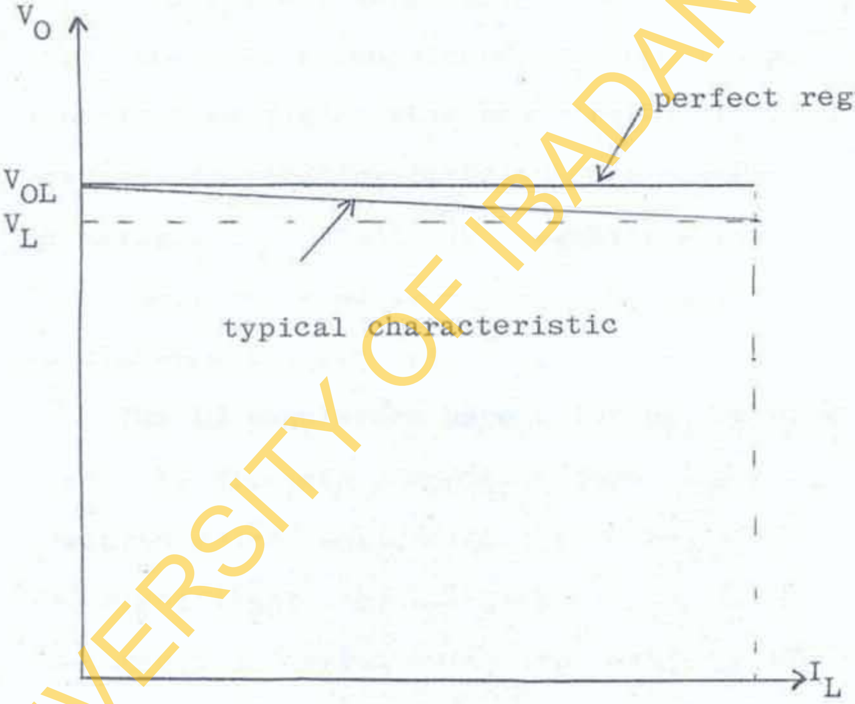


Fig. 8: Regulated voltage characteristics.

The amount of regulation in percentage is given by,

$$\% \text{ regulation} = \frac{V_{OL} - V_L}{V_L} \times 100\% \quad — \quad (9).$$

But $V_L = I_L R_L$, there fire,

$$\% \text{ regulation} = \frac{V_{OL} - V_L}{I_L R_L} \times 100\% \quad — \quad (10).$$

The output resistance, R_O, of the regulator circuit is given by,

$$R_O = \frac{V_{OL} - V_L}{I_L} \qquad — (11)$$

$\therefore$ Eqn. 10 can be rewritten as;

$$\% \text{ regulation} = \frac{R_O}{R_L} \times 100\% \qquad — (12).$$

Therefore, for a given load, regulation improves as:

(i) the voltage deviation, $V_{OL} - V_L$ is small and;

(ii) the output resistance, R_O, becomes smaller.

A perfect regulator then has zero output resistance. Low cost fabricating techniques have made a large number of integrated circuit (IC) regulators available commercially. These devices range from fairly simple, fixed-voltage types to high-quality precision regulators.

The IC regulators have a lot of features built into them. In discrete components form, implementing these features would require a lot of extra space, complexity and significant increase in cost. Among the IC regulator features are: current limiting, self protection against excessive heating, remote control, remote shut-down, operation over a wide range of input voltages, and foldback current limiting.

The various types of IC voltage regulators are:

(i) Group of fixed positive-voltage regulators in series 78xx. Fig. 9a shows the connections of the regulator. ViN is the output of the rectifier-filter circuits, and capacitors C_1 and C_2 help to maintain the dc voltage and act as additional filter for any high frequency voltage variation. Table 3 lists some typical data.

(ii) Negative voltage regulator ICs are available in series 79xx (Fig. 9b). Table 4 lists the 79xx series typical data.

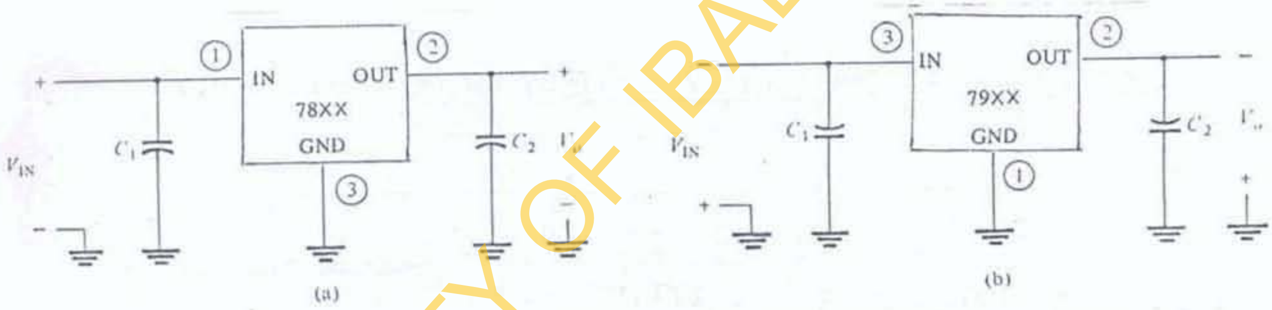


Fig. 9: (a) Series 78xx positive-voltage regulator;
(b) Series 79xx negative-voltage regulator.

(iii) IC voltage regulators that allow the user to set the output voltage to a desired regulated value. The LM 317 (Fig. 10), for example, can be operated with output voltage regulated at any setting over the range of 1.2V to 37V, by the appropriate selection of resistors R_1 and R_2.

The negative equivalent is the LM337.

Table 3 [7] : Positive Series 78xx Voltage Regulator IC

IC Part Number	Regulated Output Voltage (V)	Minimum Vin (V)
7805	+5	7.3
7806	+6	8.35
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21
7824	+24	27.1

Table 4 [7] : Fixed-Negative-Voltage Regulators in 79xx Series

IC Part Number	Regulated Output Voltage (V)	Minimum Vin (V)
7905	-5	-7.3
7906	-6	-8.4
7908	-8	-10.5
7909	-9	-11.5
7912	-12	-14.6
7915	-15	-17.7
7918	-18	-20.8
7924	-24	-27.1

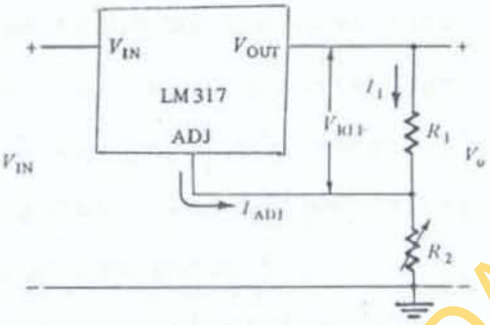


Fig. 10: Connection of LM317 adjustable-voltage regulator.

3.4 Power Supplies Design

The transformer design to meet the power supplies specifications; ±5V, ±12V as well as variable voltages of 0-40V and 0- -35V, has been done in section 2.

For the ±5V supply, the minimum dc voltage, V_{IN} (Tables 3 and 4) required at the input terminal of the 7805 and 7905 regulators are ±7.3V.

For a 2% ripple voltage for instance,

$$V_{r(rms)} = 0.02V_{dc}$$

$$V_{rpeak} = \sqrt{3}\, V_{rms} = 0.0346V_{dc}.$$

From Eqn. 3,

$$V_{IN} = Vdc = Vm - Vrpeak$$

$$Vdc = 0.97Vm \geqq \pm 7.3V$$

$$\text{hence } Vm \geqq 7.55V.$$

The transformer design in section 2 was carried out for $V_m = 9V$ (18V centre-tapped for ±5V) as indicated in Table 2, resulting in Vdc value of 8.73V.

Hence $V_{r(rms)} = 0.175V$.

For a full load current of I = 1A, then from Eqn. 7, the value of the capacitor required is, C = 16610µF. This is quite high, as choosing a value of 4700µF will give a ripple factor of 7% at full load; a rare operating point. The bridge diodes are chosen by the following design guide:

(i) Since each of the 78xx and 79xx regulator output current is rated 1A, then a diode with $I_{av} \geq 2A$ was chosen.

(ii) The PIV of the diode is given by,

$PIV > 120\% \; V_{dcNL}$.

For a ±5V dual power supply,

$V_{dcN} = 2x9V = 18V$

$\therefore PIV \geq 21.6V$.

Similar calculations were made for other supplies and the component specifications are given in Table 5. for the overall power supply circuit.

TABLE 5: COMPONENT SPECIFICATIONS

Power Supply	Diode Rectifiers	Electrolytic Filter Capacitors	Regulator Type
Fixed ±5V,1A	IN5401 100V,3A	4700µF 50WVDC*	7805/ 7905
Fixed ±12V,1A	IN5401 100V,3A	6800µF 63WVDC	7812/ 7912
Variable 0-40V,1.5A	PBL406 220V,5A	6800µF 63WVDC	LM317
Variable 0- -35V,1.5A	PBL406, 220V,5A	6800µF 63WVDC	LM337

* WVDC - Working Volts DC.

The complete circuit diagram (Fig. 11) is housed in a wooden box frame with provision for natural air cooling of the transformer. Fig. 12 is the photographic picture of the module.

4. CONCLUSION

The designand construction of an appropriate transformer formed the backbone of the design of the power supply, and of course, is responsible for the success of this work.

The specifications are fixed voltages of ±5V, ±12V, variable voltages 0-40V and 0- -35V, with protective circuits incorporated.

The module is similar to having six power supply units.

The overall objective of producing a durable unit that can withstand the test of students' rugged usage in the laboratory has been achieved. The device is now in use in our laboratory.

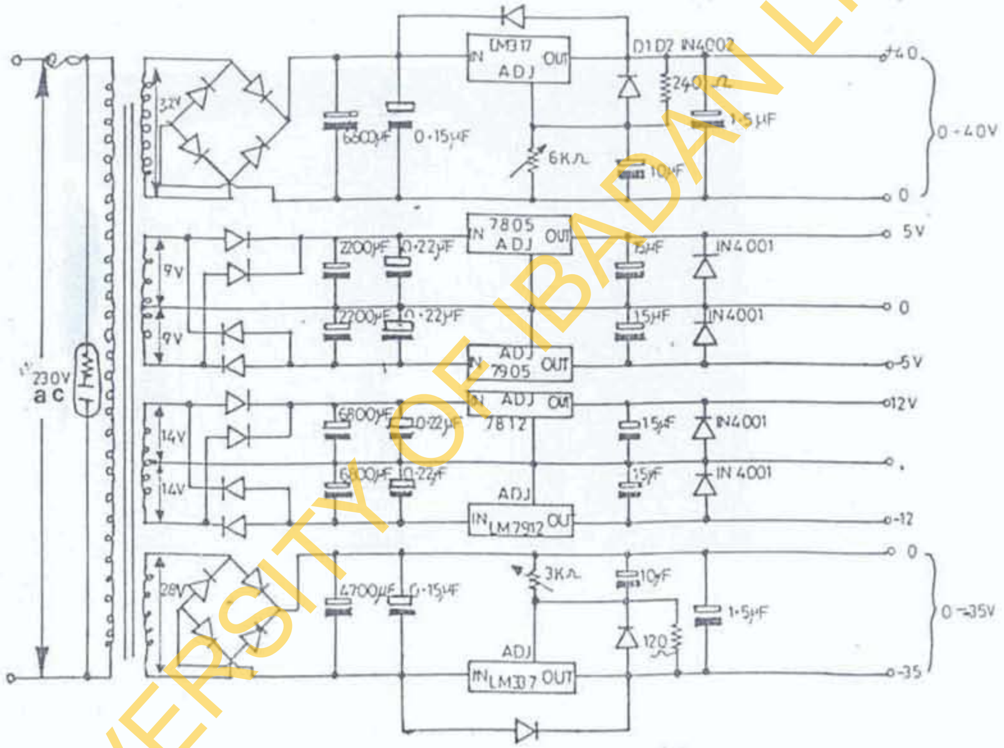

230V
a c
32V
9V
9V
14V
14V
28V
6800μF
0·15μF
LM317
IN
ADJ
OUT
D1 D2 IN4002
240 Ω
1·5μF
6KΩ
10μF
+40
0-40V
0
2200μF
0·22μF
7805
15μF
IN4001
5V
0
-5V
7905
12V
6800μF
0·22μF
7812
15μF
IN4001
IN 4001
-12
LM7912
0
4700μF
0·15μF
3KΩ
10μF
120
1·5μF
0-35V
LM337
-35

Fig. 11: COMPLETE CIRCUIT DIAGRAM.

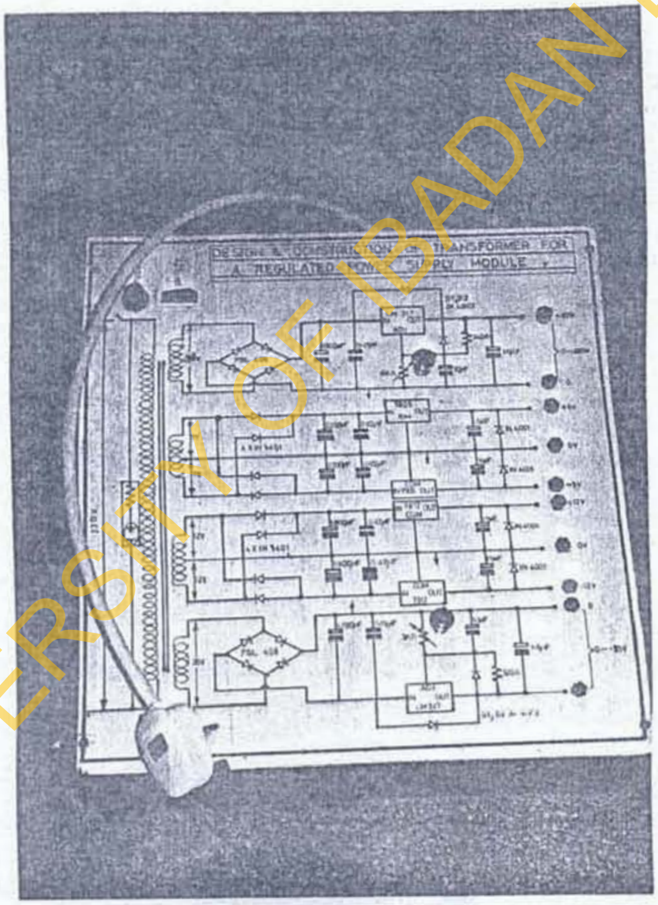

DESIGN & CONSTRUCTION OF TRANSFORMER FOR
A REGULATED POWER SUPPLY MODULE

Fig. 12: THE MODULE.

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APPENDIX III (1994)

SCR SPEED CONTROL OF DC SHUNT MOTOR

1. INTRODUCTION

The role and importance of the speed control of d.c motors in industrial set-ups and laboratories cannot be overemphasized. It readily finds applications in such areas as handtools, foodmixers, washing machines and the conveyor belt drives. Motors have to be started, run up to operating speed and stopped in normal duty or in emergency.

Speeds may have to be fairly constant and accurate for certain operations. These include the paper-making process where accurate speed control is essential. At the pulp end the mix is very wet (99% moisture) and tender; at the reeling end it is strong and nearly dry (9% moisture). Between these two extremes, the paper passes through a series of rolls, driven by up to a score of motors. To avoid tearing, all motors must run at carefully adjusted and interrelated speeds. However, to permit for the production of different paper qualities, overall speeds must be adjustable. Other applications are in the rolling-mills, mine winder and conveyor belt used in production lines.

Speed control of d.c motors can be achieved in a lot of ways, however, only few of them are practically and economically viable. Among the earliest methods used for the speed control of d.c motors is the Ward-Leonard system. It is one of the most versatile methods and involves the use of a separate motor-generator set to supply variable voltage to the armature of the machine under control while its field is supplied with a fixed voltage. The motor is usually a 3-phase squirrel-cage induction motor driving the separately excited d.c generator. The major constraint of this system lies in its size and cost considerations. Other methods include the use of a power transistor operated in the switching (ON/OFF) mode. With typical output of 100A and a forward voltage drop of 1-2V, for turn-off, the base current must be reversed, the non conduction state being achieved in about 10μS. Such very rapid rates of change of current and voltage make the design of the circuit layout critical.

Considering the constraints associated with the already mentioned methods and the need for an effective speed control at reasonable cost, the advent of thyristors in the early 1960s can be referred to as a blessing. The main advantage of thyristor is their ability to control large amounts of load power with a very minimal expenditure of control power. For the power transistor, a high and continuous base current is required for it to be held in saturation.

For example, a 50A transistor requires 1.0A of base current at 0.7V, V_{BE}, while the thyristor will be triggered into conduction by 1.5V, 50mA gate pulse.

The silicon-controlled rectifier (SCR) is a member of the thyristor family. It is one of the oldest and by far the most used in the family. The rating of the SCR is usually given in rms values, typically 1-300A average anode current at 25-1200V voltage.

In the design and construction of the laboratory equipment, size, cost and expended power are some of the factors considered. The task at hand, therefore, is to produce a module which will facilitate the speed control of d.c shunt motors using the SCR (open loop method). The module is expected to be used in the laboratory, among other things, to augment the teachings of power-electronics in the use of thyristors, and hence bridge the gap between theory and practice.

2. DESIGN CONSIDERATIONS

As already stated, that motor speed has to be adjustable to suit the various applications mentioned in Section 1. For the problem at hand, a d.c shunt motor is to be controlled using the SCR (open loop method).

2.1 D.C Shunt Motor

The arrangement of a shunt motor is given in schematic form as in Fig. 1 with the field winding connected in parallel with the armature.

The shunt motor is essentially a constant speed machine with a low speed regulation. An electric motor must produce rotation of a shaft against a load torgue. The electromagnetic torgue, Te, produced by a shunt motor is given by:

$$T_e = K\Phi I_a = K_m I_a \quad \text{—— (1)}$$

where K - machine constant, Φ the flux per pole, I_a the armature current, and K_m the machine constant for a constant flux.

The generated emf, E, is expressed as,

$$E = K\Phi w = K_m w \quad \text{—— (2)}$$

where w is the angular frequency.

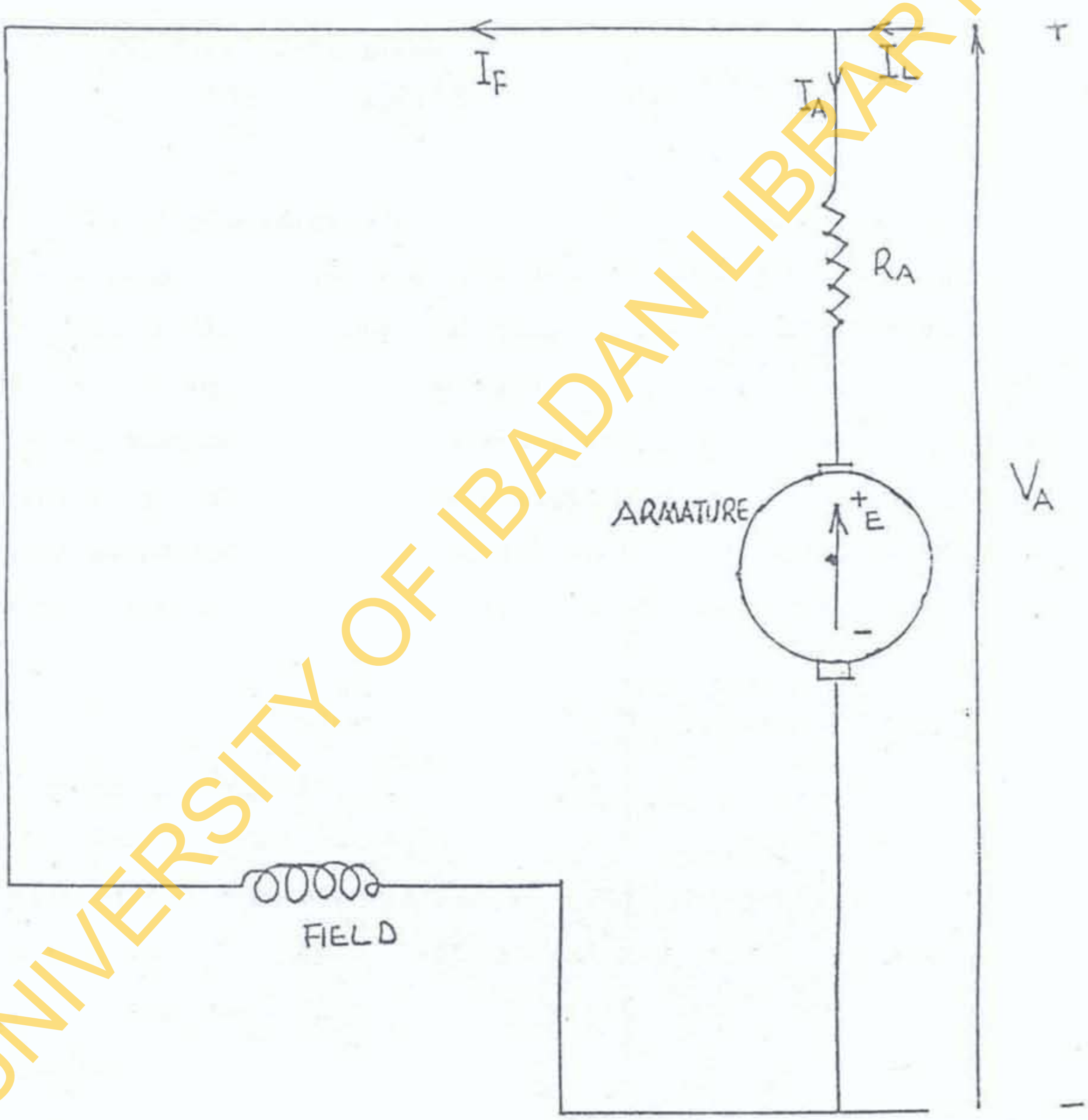
I_F
I_A
I_L
R_A
ARMATURE
+
E
−
V_A
+
−
FIELD

Fig. 1: Schematic Diagram for a Shunt Motor.

For a motor, the terminal voltage, V, is expressed as;

$$V = E+I_aR_a \qquad \text{——} \qquad (3)$$

I_a being the armature current.

Combining Eqns. 1-3, gives

$$T_e = \frac{K\Phi V}{R_a} - \frac{(K\Phi)^2 w}{R_a} \qquad \text{——} \qquad (4).$$

The implication of Equation 4 is that the speed of an electric motor could be controlled by varying the voltage applied to the armature, the flux, and the armature resistance. Though Eqn. 4 shows that the speed could be controlled by varying the armature resistance, this approach is generally undesirable since energy is wasted. Therefore, all methods of speed control should involve the variation of either the armature voltage or flux, or both of these parameters.

2.2 Design Layout

Based on the established fact that varying either the flux or the armature voltage can alter the speed of a d.c motor, an open-loop control system (Fig. 2) is employed, whereby the terminal voltage is varied and consequently varying the motor speed.

The controller is a silicon controlled rectifier (SCR), while the control logic system block is a means of controlling the SCR, i.e., the firing circuit. The control logic system has the same source of power as the motor armature circuit for synchronization purposes.

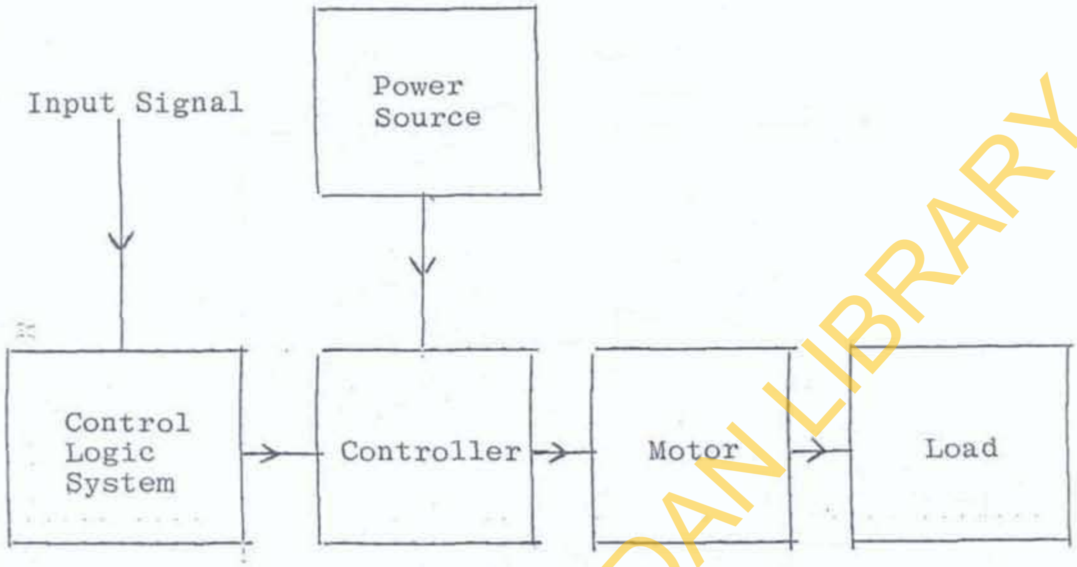
Input Signal
Power Source
Control Logic System
Controller
Motor
Load

Fig. 2: Basic Scheme of Electronic Motor Control.

2.3 Design Specifications

The motor speed control circuit specifications are:

(i) Synchronization of the firing circuit with the armature circuit, especially in frequency and phase;

(ii) Optima operation of the SCR; and

(iii) Easy control of the motor in all load conditions.

2.4 Design Realization

The control circuit is as shown in Fig. 3. The passive and active components are listed in Table 1. These values were chosen to meet the design specifications.

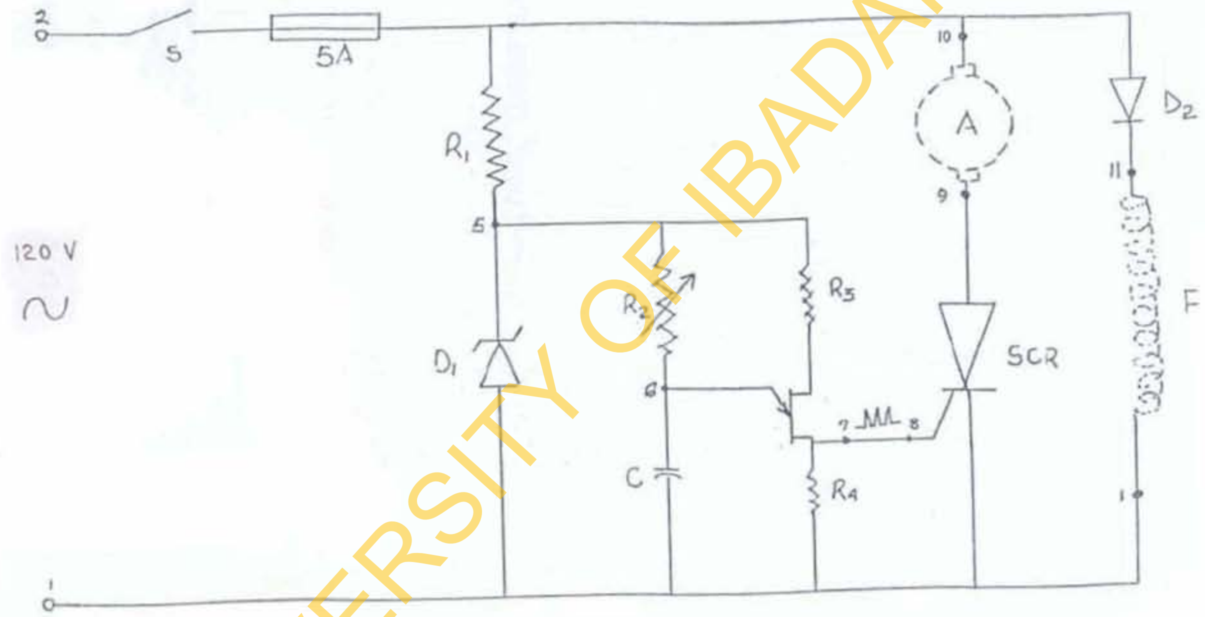
2
S
5A
R₁
5
R₂
6
R₃
10
A
9
D₂
11
120 V
~
D₁
SCR
7
8
C
R₄
F
1
1

Fig. 3: The Complete Circuit Diagram.

Table 1: Components Used in the Control Circuit.

Components	Types
RESISTORS:	
R_1	13KΩ, 10W
R_2 (variable)	5KΩ, ½W
R_3	2KΩ, ¼W
R_4	6.8Ω, 5W
R_5	10Ω, 5W
CAPACITOR, C	0.1μF, 600V
DIODES:	
D_1	30V Zener
D_2	600V
Uninjunction Transistor (UJT)	2N2646
SCR	BTY 79-400R

2.4.1 Power Supply Requirements

A variac is used to step down the mains voltage to the required 120V a.c.

The firing circuit requires 30V d.c power supply. This is obtained from the power resistor, R_1 and the 30V zener diode D_1 combination. R_1 acts as a current limiting device.

The power supply to the load, which is the shunt motor, is in two folds: a constant supply to the field windings; while the other is the variable power supply to the armature circuit. The constant supply to the field winding is by means of diode D_2 which produces half-wave rectified average voltage V_f across the field winding.

2.4.2 The Firing Circuit

The firing circuit is of immense importance to the overall control circuit. The firing circuit is as shown in Fig. 4. The variable resistor R_2 is used to vary the time constant, τ, for the charging and discharging of the capacitor, and hence the resulting electrical pulses of the firing circuit is varied. By knowing the time of the first pulse, the firing angle can be determined from the expression;

$$\theta = 18t \qquad \text{——} \quad (5).$$

2.4.3 The SCR

The BTY 79-400R SCR ratings; voltage, current, power and temperature, were the determining factors in employing the device for the design purpose.

The constraint on maximum operating temperature was met by the appropriate choice of a heat sink. The heat sink rapidly dissipates heat from the SCR. The one used, for this project, has a thermal resistance of 2.1°C/W and the dimensions are $12 \times 8 \times 2.5\text{cm}^3$.

The major protection, apart from optima application of the SCR, is the 5A line surge fuse (Fig. 3). A surge fuse responds to surges, making it more sensitive than the conventional fuses.

The whole circuit is housed in a wooden box frame having dimension 37cm x 35cm x 12cm.

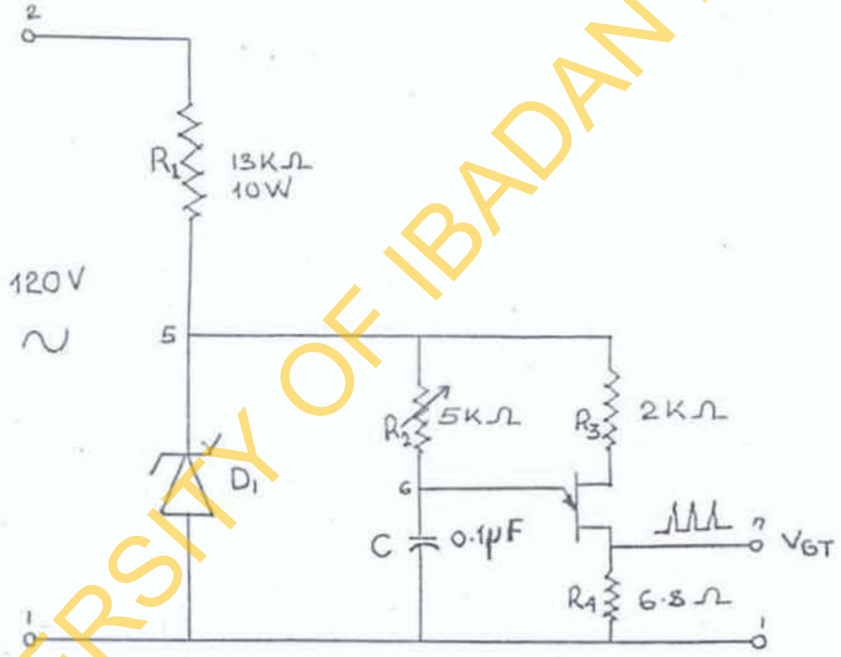
2
R1
13KΩ
10W
120V
∿
5
R2
5KΩ
R3
2KΩ
D1
6
C
0.1μF
7
VGT
R4
6.8Ω
1
1

Fig. 4: The Basic Firing Circuit.

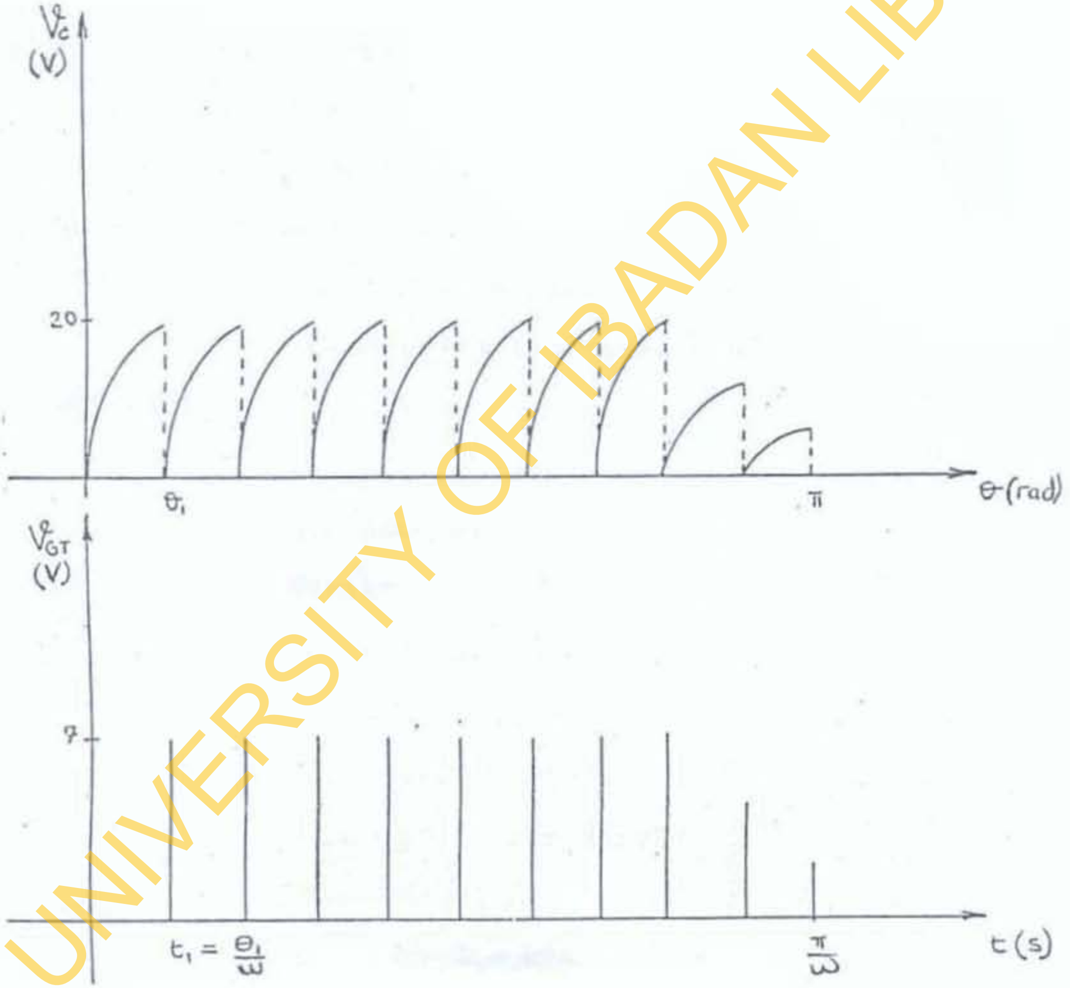

Fig. 5: Capacitor and Output Pulse Waveforms.

3. INSTRUCTIONAL MANUAL:

The performance of the circuit was tested by following the procedure outlined in this section.

Once the circuit connections have been made, the next step is to proceed with the experiment as indicated in the instructional manual. The experimental procedure outlines the necessary steps to be taken during the experiment. It is important to note here that the user must adhere strictly to all the instructions in this manual.

The experiment on d.c shunt motor speed control is carried out as follows:

AIM : To study the open loop control of a d.c shunt motor using the circuit of Fig. 3.

EQUIPMENT: Digital Voltmeter
Dual-trace oscilloscope
A.C Ammeter
Variac
Connecting leads
The SCR speed control Module
D.C machine EM8211
Hand Tachometer EM8920

THEORY : There are different methods of controlling the speed of d.c shunt motors. Some of these are: Application of variable armature voltages, varying the armature current and varying the field current. The SCR acts both as a rectifier and a variable voltage source, by varying its firing angle, θ. This intrinsic advantage of the SCR to supply variable average voltages is employed in the SCR control of the d.c shunt motor. The d.c machine EM8211 is used for this experiment. The open loop speed controller consists of a field supply and a varying armature power supply.

PROCEDURE

(1) Set R_2 completely clockwise, for maximum resistance.

(2) Connect up the circuit in Fig. 3.

(3) Connect terminals 7 and 8 together so that the triggering signal from the firing circuit can be applied to the gate of the SCR.

(4) Observe the capacitor voltage Vc and the resulting firing pulses by connecting the dual-trace oscilloscope to terminals 6 and 7.

(5) Turn on the power supply.

(6) Adjust R_2 until the motor just rotates. Record the triggering time, t_1. (Given by Equation 5).

(7) Repeat step 6 above for motor speeds up to 1500rpm by using a hand tachometer, taking up to five readings. Record the corresponding triggering time, t.

RESULTS

(1) Draw the observed waveforms for the capacitor voltage Vc and the triggering voltage V_{GT}.

(2) Calculate the firing angle, θ, from the relation

$$\theta = 18t$$

(3) Plot the graph of speed (r.p.m) against $\theta(^{o}C)$.

(4) Comment on your results.

4. CONCLUSION:

The aim of this work has been to build a laboratory module which controls the speed of a d.c shunt motor. In the process, the BTY79 - 400R SCR has been employed.

The speed of a ¼ H.P laboratory machine EM8211 has been effectively controlled using the SCR. The UJT (2N2646), is the major component in the firing circuit, produces 8 pulses at peak voltage of 7V in one half-cycle. With the module, the speed variation of the d.c shunt motor (EM8211) was from 0 to 1600 r.p.m. An instructional manual is provided in Section 3 to aid in the usage of the module.